Design of An Adaptive Router Architecture for Network-on-Chip

Seung Eun Lee and Jun Ho Bahn

Nader Bagherzadeh, Dept. of Electrical Engineering and Computer Science

The Henry Samueli School of Engineering, UC Irvine

University of California, Irvine

Abstract *– An adaptive router architecture for a flexible on-chip interconnection is proposed and applied to the Macro-pipelined Reconfigurable System (MaRS) as an interconnection method. It adopts a wormhole switching technique and its routing algorithm is livelock-/deadlock-free in 2-D mesh topology. Major contributions of this research are the design of Network-on-Chip (NoC) architecture adopting a minimal adaptive routing algorithm with near-optimal performance and feasible design complexity, thus satisfying general SoC design requirements. By providing a consistent way of constructing network architecture in 2-D mesh topology, it guarantees scalability and can be applied to different SoC design environment. To prove the router performance and its feasibility for VLSI implementation, the adaptive router is synthesized using TSMC™ 90nm standard CMOS technology. The bandwidth of the router and the total area overhead make the proposed router feasible for NoC.*

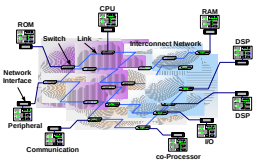
Keyword *- Network-on-Chip (NoC), System-on-Chip (SoC), Macro-pipelined Reconfigurable System (MaRS)*

1 Introduction

- The scaling down of transistor size is providing opportunities to have a large number of IPs integrated on a single chip
- Moreover Time-to-Market needs to be kept as low as possible
- The interconnection among multiple IPs becomes another challenging issue in System-on-Chip (SoC) design
- The use of packet switching for on-chip interconnection network was proposed → Network-on-Chip (NoC)
- The router in NoC has tight resource constraints
  - Simple and light-weighted functionality
  - Small area, low power, and high speed
  - High-throughput in communication

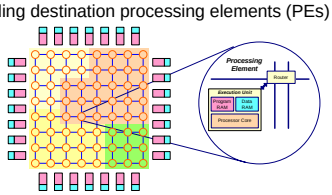
2 Network-on-Chip

- Communication resources are shared instead of creating a dedicated channel between each terminal pair
- Bandwidth is enhanced by sharing network channels
- Regularity allows layering and reuse of communication resources
- Short wire segmentation allows low energy dissipation
- NoC provides opportunities for scalability and freedom from the limitation of complex wiring



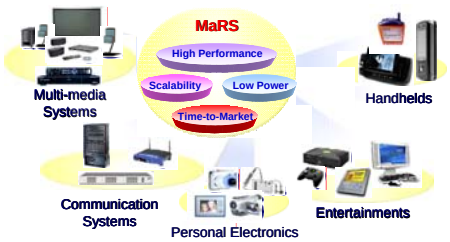
3 Macro-pipelined Reconfigurable System

- 2D-mesh topology of processing elements (PEs)
- All data processing tasks are performed in the execution unit (EU)
- The router is in charge of directing the ongoing traffic toward the corresponding destination processing elements (PEs)



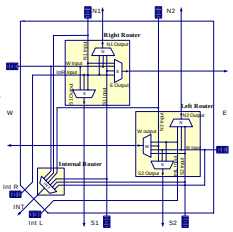
4 Application Fields

- Computation/data intensive signal processing



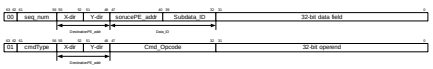
5 Adaptive Router Architecture

- Minimal adaptive routing based on wormhole switching technique guaranteeing livelock-/deadlock-freedom
- Point-to-point single or block transfer
- Two disjoint sub-networks for the west-to-east and east-to-west traffics
  - Network avoids a cyclic dependency, resulting in deadlock-freedom

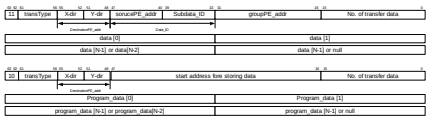


6 Packet Format

- Single Data/Command Transfer Packet

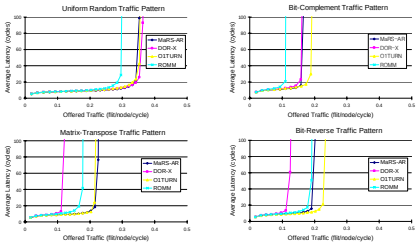


- Block Program/Data Transfer Packet



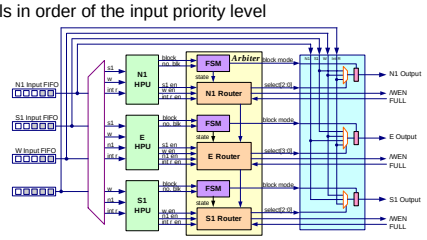
7 Performance Comparison

- The proposed adaptive routing algorithm has near-optimal performance with comparison to O1TURN



8 Design of Prototype Router

- The sub-routers for each output port are placed according to its priority
- The Header Parsing Unit (HPU) generates a set of corresponding signals in order of the input priority level



9 Physical Implementation

- Description: Verilog™ HDL
- Synthesis: Synopsys™ V-2003.12.
- Technology: TSMC™ 90 *nm* standard CMOS

	Router	FIFO (depth=4)
Operating Voltage	1.0V	1.0 V
Operating Frequency	423 *MHz*	1.8 *GHz*
Area	17,537 μm^2	8,384 μm^2
Dynamic Power	2.4680 *mW*	5.3338 *mW*
Leakage Power	171.9375 μW	77.2560 μW

10 Conclusions

- Introduced NoC as an interconnection network for SoC design
- Proposed a near-optimal adaptive routing algorithm
- Implemented a prototype router
- Average latency in 8×8 network with uniform random traffic pattern
  - 32-depth FIFO shows optimal performance in terms of latency
  - Considering area and power, 4-depth FIFO is enough
- Demonstrated the feasibility of the router for NoC
  - Bandwidth, area overhead, and power consumption
- The proposed adaptive router is a feasible solution for on-chip interconnection in state-of-art SoC design such as Giga-scale SoC, Chip-Multi-Processor (CMP)

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