TSV-to-TSV Inductive Coupling-Aware Coding Scheme for 3D Network-on-Chip

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***Abstract*—A reliable Three Dimensional Network-on-Chip (3D NoC) is required for future many-core systems. Through-silicon Via (TSV) is the prominent component of 3D NoC to support better performance and lower power consumption. Inductive TSV coupling has large disruptive effects on Signal Integrity (SI) and transmission delay. In this paper, TSV inductive coupling is analyzed based on technology process, TSV length, and TSV radius for a range of frequencies. A classification of inductive coupling voltage is presented for different TSV configurations. A novel coding technique is devised to mitigate the inductive coupling effects by adjusting the current flow pattern. Simulations for a 4×8 TSV matrix show 23% coupled voltage mitigation, imposing 12.5% information redundancy.**

I. Introduction

The fast IC development has been scaled down because of physical limitations; employing many-core designs instead of a single core with higher frequency has been proposed. Network-on-Chip (NoC) as a network of routers has been suggested to implement the connectivity of these cores [1], [2]. Many different on-chip communication methods have been introduced such as on-chip optical switches [3] to support higher data transmission rate. However, they all have undesirable overheads like electrical to optical conversion. Three Dimensional (3D) design is the best promising approach for next generation of many-core integration on a chip, while imposing smaller footprint area and better timing performance than 2D architecture [4]. The combination of 3D integration and NoC technologies provides a new horizon for on-chip interconnect design. 3D NoC offers higher bandwidth, smaller form factor, shorter wire length, lower power dissipation, and better performance than traditional 2D NoCs [5]. 3D integration by Through-silicon Via (TSV) is currently the most popular choice as a vertical-electrical connection form between tiers which is demonstrated in Fig. 1. However, they suffer from physical faults such as chip warpage, TSV coupling, and thermal stress [6], [7]. Signal Integrity (SI) effect is another key challenge in 3D ICs with TSVs (sources of coupling noise), resulting in path delay extension [8], [9].

On the other hand, fault occurrence rate increases with feature size reduction of logic devices [10], which will be worsen for 3D stacked designs. Many fault tolerance assessment and fault-tolerant methods have been experimented to present reliable 2D NoCs [2]. A fault-tolerant 2D NoC router is presented in [11] in which routing table and switch component are capable of handling SEU and SET faults.

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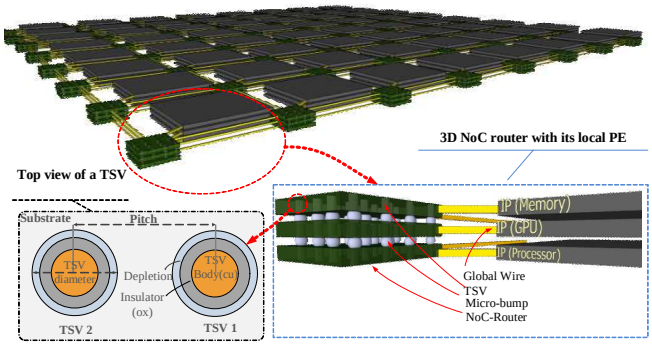
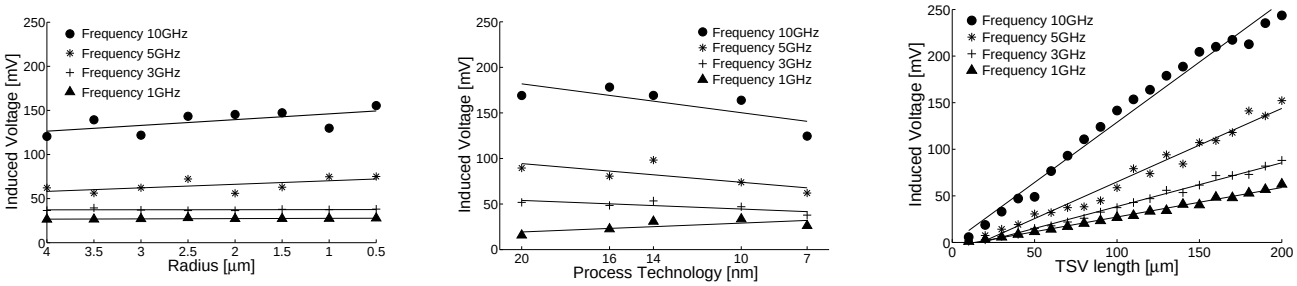


Fig. 1. Stacked 2D planar, vertically interconnected by TSVs in 3D integration technology

However, new challenges of 3D designs remind the reliability concerns for 3D NoC designs as petascale computational performance comes to fruition. An analytical model for the coupling capacitance between pairs of TSVs is reported in [9]. Five solutions are suggested in [12] to reduce the coupling including: increasing TSV distances, shielding the victim TSVs, inserting buffers at the victim net, decreasing the driver size at the aggressor net, and increasing the load at both victim and aggressor net. The last two approaches have negative implications for timing performance, and others need high effort at post-design time. A coding scheme has been suggested for a matrix of TSVs, reducing the maximum crosstalk by 25% [8]. However, this approach is only applicable for capacitive crosstalk (coupling) and only supports a mesh of TSVs with size of $3 \times n$, limiting the TSV insertion process. It imposes around 40% information redundancy with an encoder and decoder of quadratic complexity in circuit area. However, the impact of inductive coupling on SI has not been evaluated yet. The goal of this paper is to propose a coding method in order to mitigate the inductive coupling effect on victim TSVs. The major contributions of this article are:

- To perform a circuit-level analysis of inductive TSV-to-TSV coupling effect in a 3D NoC design and to present an analytical failure estimation of TSV links caused by inductive TSV coupling effect, reported in Section II.
- To propose a scalable TSV-to-TSV coupling fault prevention coding, presented in Section III.
- To evaluate the efficiency of the proposed coding method in minimizing the inductive TSV-to-TSV coupling effect, reported in Section IV.



(a) TSV radius (b) Technology (c) TSV length

Fig. 2. HSPICE simulation results of Induced voltage in terms on TSV radius, TSV technology, and TSV length

II. Inductive Coupling Analysis

The impact of sub-micron TSVs on future 3D ICs is still unknown [13]. Inductive coupling as one of the major issues in TSV-based 3D NoC architectures is analyzed in this section. The term TSV coupling refers to capacitive and inductive couplings among neighboring TSVs. Electric field results in capacitance coupling and magnetic field is a source of inductive coupling. The capacitance coupling between TSVs depends on the permittivity of the oxide, TSV geometry, the arrangement of surrounding TSVs, and body contacts places. Inductive coupling among neighboring TSVs is more critical in higher frequency data transmissions [14], which is considered in this article.

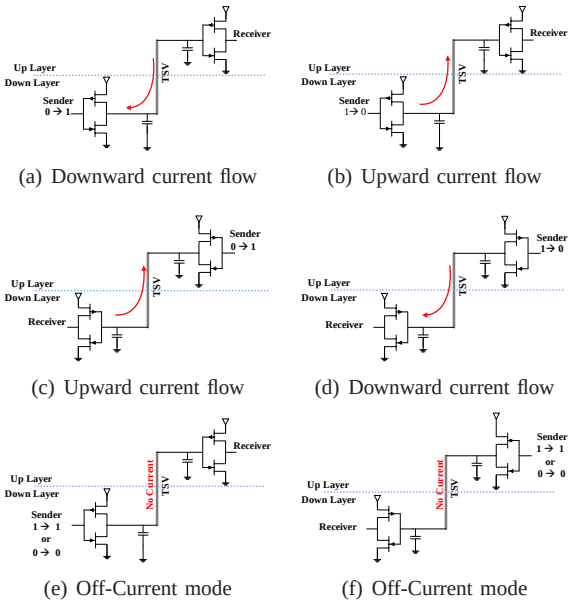
A. Inductive Coupling Characteristics

To evaluate the effect of inductive coupling, a 3×3 array of TSVs is modeled in HSPICE. The middle TSV is the victim and the other 8 are the aggressors. In simulations, the top end of each TSV is connected to the output of an inverter, which drives the input of another inverter connected to the bottom of the TSV. Predictive Technology Model (PTM) [15] FinFET transistor models are employed to implement inverters in this experiment. The worst-case induced voltage on the victim TSV is reported as regression lines for different TSV radii (Fig. 2(a)), process technologies (Fig. 2(b)), and TSV lengths (Fig. 2(c)) over different frequencies. The range of all of these parameters are chosen according to ITRS [7] interconnect report.

The minimum height of global TSVs cannot be less than $20-50\mu m$ earlier than 2018 based on ITRS [7]. A copper TSV in standard Si-bulk technology normally has via diameter of $2\mu m$-$8\mu m$ (by 2018), $5\mu m$ by $5\mu m$ contact pads, $4\mu m$-$16\mu m$ via pitch, $0.5\mu m$ oxide thickness (t_{ox}), and $20\mu m$-$50\mu m$ layer thickness, including substrate and metallization [7]. TSV process is independent of the 2D chip design technology. TSV diameters are two to three orders of magnitude more than transistor wire lengths. The maximum delay of a TSV with the length of $50\mu m$ is approximated to be $10ps$ [16]. As TSVs become longer the magnetic flux linking the two TSVs increases proportionally. So the coupling voltage between victim and aggressor TSVs and hence the total inductive coupled voltage rise by increasing the length of TSVs (see Fig. 2(c)). Although the linkage flux between two TSVs is a strong function of the length, its dependence to radius is very weak. Changing the radius of cylindrical TSVs affects mutual inductance by changing the magnetic field because of TSV aggressors and the exposed surface to the linkage flux. As long as the current distribution in a TSV remains almost symmetric, assuming proximity effect and other high order effects are trivial, the magnetic field created by an aggressor is almost constant. In other words, the TSV radius changes effect on the magnetic field of TSVs is not critical. Since the length of the TSV is at least an order of magnitude larger than its radius, the second effect is small, however the linkage flux and consequently mutual coupling decreases slightly as radius increases (see Fig. 2(a)). As shown in Fig. 2(b), induced voltage is a weak function of the process technology. As processes advance, gate capacitance gets smaller and at the same time rise time and fall time of voltages become shorter. Overall the charging and discharging current of gate capacitance remains almost constant. The same current that charges (or discharges) the gate capacitance passes through TSV and causes inductive coupling to neighboring TSVs. Thus, inductively coupled voltage remains almost constant for different technologies. As technology advances and supply voltage shrinks, the coupled voltage becomes a greater portion of V_{dd} and increases the probability of error. Consequently, the length of TSVs has the major impact on inductive coupling, resulting in unexpected noises in 3D NoC as the number of layers increases.

B. Current Flow in TSVs

The current flow direction of a TSV is data-dependent, based on charging and discharging of the intermediate capacitor between each pair of transistors of stacked planar. The behavior of the intermediate capacitor relies on the previous and current data bit values. Fig. 3 illustrates six possible cases depending on the data bit values and location of the sender, resulting in three possible current flows in TSVs. There is a downward current flow when the input data bit of sender changes from '0' to '1' and '1' to '0' if the sender is in lower and upper level respectively as shown in Fig. 3(a) and Fig. 3(d). Similarly, there is an upward current flow direction, if the data bit of the sender changes from '1' to '0' and '0' to '1' if the sender is in lower and upper level respectively



(a) Downward current flow (b) Upward current flow

(c) Upward current flow (d) Downward current flow

(e) Off-Current mode (f) Off-Current mode

Fig. 3. Current flow direction in TSV.

as shown in Fig. 3(b) and Fig. 3(c). TSV does not carry any current, if there is no switching between the previous and next data bit values, as showed in Fig. 3(e) and Fig. 3(f). In the rest of this article such a TSV is called an inactive TSV, which does not have any current flow.

III. Proposed Coding Algorithm

There are different current flow patterns in which the effect of inductive coupling will be negligible. As an example assume a current flow pattern in which the previous sent data bits are exactly same as the following data bits; in this case there is no current flows in TSVs. However, the probability of reaching these patterns is very low. An ideal TSV-to-TSV inductive coupling aware approach must handle any current flow pattern, while not adversely affecting the desirable patterns. A coding scheme is proposed in Subsection III-B to support all possible current flow patterns.

A. Problem Definition

TSV coupling is a major source of noise when at least two neighboring TSVs are transferring data simultaneously.

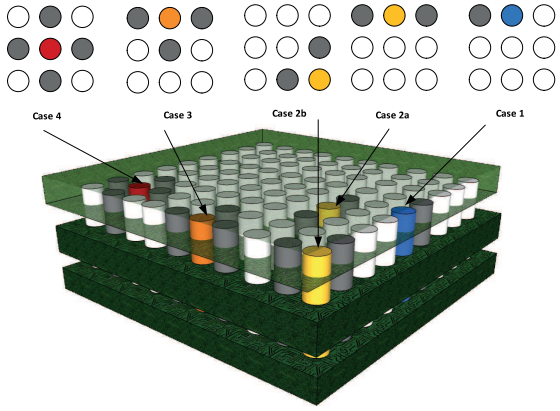


Fig. 4. Different TSV patterns leading to inductive coupling

TABLE I
TSV-TSV Inductive Coupling Failure Analysis

Case	$\lvert\alpha\rvert$	Basic Patterns	Similar patterns
—	0	⊕	1
1	1	⊕ ⊙	8
2	2	⊙ ⊕ ⊙	12
	0	⊙ ⊕ ⊗	12
3	3	⊙ ⊙ ⊕ ⊙	8
	1	⊙ ⊙ ⊕ ⊗	24
4	4	⊙ ⊙ ⊕ ⊙ ⊙	2
	0	⊗ ⊙ ⊕ ⊙ ⊗	6
	2	⊙ ⊙ ⊕ ⊙ ⊗	8

With the cross section view of TSVs, it is assumed that only vertical or horizontal adjacent TSVs have mutual coupling effect on each other. The effect of diagonal neighboring TSVs, which has less mutual coupling effect than adjacent TSVs, is not considered here for the sake of the proposed coding efficiency. With this assumption an inductive TSV coupling is classified into four different cases based on the number and arrangement of active neighbors for a victim TSV, which are shown by a graphical pattern in Fig. 4. The colored TSVs and gray ones in Fig. 4 represent victim and aggressor TSVs, respectively. The inductively-induced coupling failure probability of a TSV is a function of the unexpected total coupled voltage ($V_{Icoupl_{tot}}$) caused by its active neighbor TSVs. Assume that the inductive coupling voltage caused by a single horizontal or vertical neighboring TSV is β; then $V_{Icoupl_{tot}}$ is proportional to $\alpha\beta$, where the value of parameter α depends on the current flow direction and arrangement of active neighboring TSVs. Assuming the electromagnetic proximity effect and other high order effects are negligible, the total inductively coupled voltage on the victim TSV is equal to sum of the voltages induced by each aggressor TSV based on Faraday's law as shown in Equation 1.

$$V_{Icoupl_{tot}} = \sum_{i=1}^{N} V_{Icoupl_i} = \sum_{i=1}^{N} M_{\mathrm{v,i}} \frac{dI_i}{dt} \sim \alpha\beta \qquad (1)$$

where N is the total number of aggressors, V_{Icoupl_i} is the voltage coupled on the victim by i^{th} aggressor, assuming all other aggressors have constant current. $M_{\mathrm{v,i}}$ is the mutual inductance between i^{th} aggressor and victim TSVs. I_i is the current of i^{th} aggressor TSV. The $M_{v,i}$ is extracted from Equation 2 [17].

$$M_{v,i} = \frac{\mu_0}{2\pi}\left[l\ln\left(\frac{l+\sqrt{{d_i}^2+l^2}}{d_i}\right) + d_i - \sqrt{{d_i}^2+l^2}\right] \qquad (2)$$

where d_i is the distance of i^{th} aggressor from the victim TSV and l is the length of a TSV. Each victim TSV has four neighbors in horizontal or vertical directions. These neighboring TSVs can be either active or inactive. An active

may have upward or downward current directions, while there is no current flow in an inactive TSV. As a result, there are $3^4 = 81$ possible configurations of TSV neighbors for a victim TSV. Since many of these 81 arrangements behave similarly as long as the α is concerned, the behavior of all 81 configurations is summarized in TABLE I. In this table five distinct coefficients are reported for all possible 81 TSV configurations. The first column shows the corresponding case number of neighboring TSV arrangements in Fig. 4. Both of $case2_a$ and $case2_b$ of Fig. 4 have similar effect on the victim TSV; they are merged in TABLE I. The absolute value of α for each of the possible patterns are shown in the second column of TABLE I. The basic pattern and number of their occurrence are presented in third and fourth columns of TABLE I, respectively. The $\odot$, $\otimes$ symbols in TABLE I represent the upward and downward TSV current flow directions, respectively. The $\oplus$ symbol is a victim TSV regardless of its current direction which does not impact our proposed analysis. To examine the exact dependency of coupling-induced failure probability, a complex magnetic analysis of neighboring TSVs is required which is out of the scope of this paper. If the coupling voltage induced by a single neighbor on the victim has a magnitude of β, the corresponding failure chance is denoted by P_β. Similarly, $P_{\beta_{\text{tot}}} = P_{\alpha\beta}$ represents the total failure chance on a victim for a given TSV neighboring configuration. Integrating the occurrence frequency of each of α values with their corresponding failure chances due to different α values is reported in Equation 3.

$$F = \frac{19}{81}P_{0\beta} + \frac{32}{81}P_{|1|\beta} + \frac{20}{81}P_{|2|\beta} + \frac{8}{81}P_{|3|\beta} + \frac{2}{81}P_{|4|\beta} \quad (3)$$

In which, $P_{0\beta} < P_{|1|\beta} < P_{|2|\beta} < P_{|3|\beta} < P_{|4|\beta}$. The goal of this article is to reduce the number of $P_{\alpha\beta}$ with larger α values by proposing a coding technique.

B. Coding Scheme

Limiting the number of TSVs on a chip and TSV placement with a safe distance approaches have been proposed to mitigate mutual coupling but they are not efficient. The main contribution of this article is to propose a coding algorithm to mitigate TSV-to-TSV inductive coupling occurrence by adjusting the sequence of data flits. This goal is not achievable for all data patterns due to intrinsic randomness property of data, therefore the purpose of the proposed coding method is to rearrange the data bits to replace the majority of $P_{\alpha\beta}$ with larger α values by $P_{\alpha\beta}$ with smaller α values. As a practical approach for data-bit adjustments, the inversion operation is chosen. Data bit inversion is done at the receiver side to retrieve the original data-bit patterns. The overhead of this method are the extra bits, to decide the inversion process at the receiver side. However, employing a bit for each of the data-bits imposes a 100% information redundancy, so in the proposed algorithm the inversion operation is done for each row with a single bit overhead.

Algorithm 1 summarizes the proposed coding method for positive α values. There is a similar algorithm for negative α values, in which all the $IMAT[i][j]$ = $BMAT[i][j]$ assignments from line 10 to line 50 of Algorithm 1 are replaced by $IMAT[i][j]$ = $\overline{BMAT}[i][j]$. AMAT and BMAT input matrices are the two consecutive data flits, which AMAT has been sent while BMAT is planned to be sent. The proposed algorithm is able to invert the values of BMAT matrix based on the values of AMAT matrix as shown in Algorithm 1. In this algorithm, first the current flow direction of each TSV is calculated by considering the data-bit pattern of the corresponding elements in AMAT and BMAT, as explained in Subsection II-B, resulting in matrix CMAT. Then, PMAT is created by adding the values of its corresponding vertical and horizontal neighbors in CMAT based on Equation 1. There is a chance of row inversion for each row if the conditions of proposed algorithm are satisfied, as shown in Algorithm 1 with the goal of replacing majority of larger values in PMAT by smaller ones. In the proposed method

Algorithm 1 Proposed coding technique algorithm

```
1: AMAT ← Sent data bits
2: BMAT ← To be sent data bits
3: CMAT ← Current flow direction of each TSV
4: PMAT ← α values in Equation 1 for each TSV
5: IMAT ← Inversion intention for each TSV
6: for each R ∈ Rows do
7:     for each C ∈ Columns do
8:         UP ← CMAT[R-1][C]
9:         DOWN ← CMAT[R+1][C]
10:        if PMAT[R][C] == 1 then
11:            if UP == 0 then
12:                IMAT[R-1][C] = BMAT[R-1][C]
13:            else
14:                IMAT[R-1][C] = 1
15:            end if
16:        else if PMAT[R][C] == 2 then
17:            if UP == −1 or DOWN == −1 then
18:                if UP == −1 then
19:                    IMAT[R-1][C] = 1
20:                else
21:                    IMAT[R+1][C] = 1
22:                end if
23:            else if UP == 1 and DOWN == 1 then
24:                IMAT[R-1][C] = 1
25:                IMAT[R+1][C] = 1
26:            else if UP == 0 and DOWN == 0 then
27:                IMAT[R-1][C] = BMAT[R-1][C]
28:                IMAT[R+1][C] = BMAT[R+1][C]
29:            else if UP == 1 and DOWN == 0 then
30:                IMAT[R-1][C] = 1
31:                IMAT[R+1][C] = BMAT[R+1][C]
32:            else if UP == 0 and DOWN == 1 then
33:                IMAT[R-1][C] = BMAT[R-1][C]
34:                IMAT[R+1][C] = 1
35:            end if
36:        else if PMAT[R][C] == 3 then
37:            if UP == 1 and DOWN == 1 then
38:                IMAT[R-1][C] == 1
39:                IMAT[R+1][C] == 1
40:            else if UP == 0 then
41:                IMAT[R+1][C] == 1
42:                IMAT[R-1][C] == BMAT[R-1][C]
43:            else
44:                IMAT[R-1][C] == 1
45:                IMAT[R+1][C] == BMAT[R+1][C]
46:            end if
47:        else if PMAT[R][C] == 4 then
48:            IMAT[R-1][C] == 1
49:            IMAT[R+1][C] == 1
50:        end if
51:    end for
52: end for
53: for each Row ∈ IMAT do
54:     Decides whether the inversion is needed or not
55: end for
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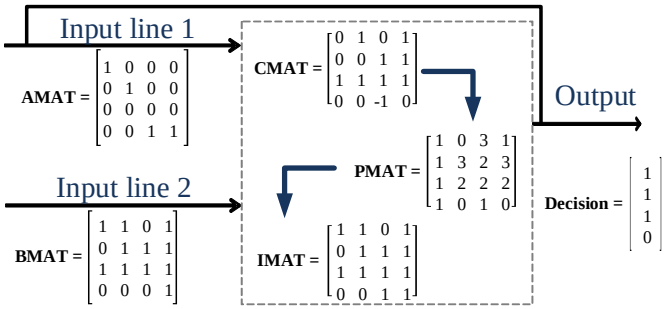


Fig. 5. 4x4 mesh of TSV example

each TSV votes for inversion of its vertical neighbors to create IMAT. The decision of inverting data pattern of adjacent rows in IMAT matrix may conflict each other, as inversion of a single row of IMAT matrix is suggested for one of its adjacent row while it is not recommended for the other one. The proposed coding algorithm addresses these dependencies and take the best decision considering the optimization of each row and their effect on the data. In this case, the net profit of inversion of each row should be calculated to find the best inverting decision for different rows of IMAT matrix. There is a trade-off between the degree of inductive coupling mitigation and performance/complexity of the design. The proposed algorithm ignores the inverting process, if there is any conflict of decision in inverting adjacent rows of IMAT matrix in order to save the timing constraints. Finally based on the number of inversion request in each row the inversion decision is made. It should be also noted that the encoding and decoding processes are only needed at source and destination Network Interfaces (NI) and since NoC routers require the header information, header flit is not encoded; B-bit (B shows the number of rows) inversion indication bits are added to the header flit of the packet to prevent imposing extra TSVs.

IV. Proposed Coding Elaboration and Evaluation

Fig. 5 illustrates an example of the proposed algorithm for given AMAT and BMAT as consecutive flits through a 4x4 mesh of TSV. Any changes from '0' to '1' in the corresponding elements of AMAT and BMAT matrices is represented as 1 in CMAT, while the reverse changes is shown by -1. A given element of CMAT will be 0 if it corresponding element in AMAT and BMAT are same. Then PMAT is generated from CMAT by adding the neighbors' values in the corresponding element of CMAT matrix. For example, the PMAT [1][1] is equal to 3, which is the summation of CMAT[0][1], CMAT[1][0], CMAT[2][1], and CMAT[1][2]. Finally, IMAT matrix is created by examining all elements of PMAT through the *if* conditions of the Algorithm 1. The values of IMAT[0][1] and IMAT[2][1] are both 1 since the condition of line 36 in Algorithm 1 (PMAT[1][1] == 3) is satisfied. The rest of values of IMAT matrix are completed by tracing the proposed algorithm. Decision vector which is sent to the receiver side is generated by voting the number of '1' values of each row in IMAT matrix. If the some of values in each row is greater than the half size of TSV array columns,

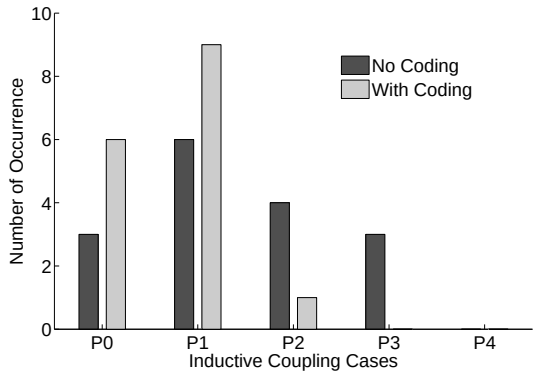
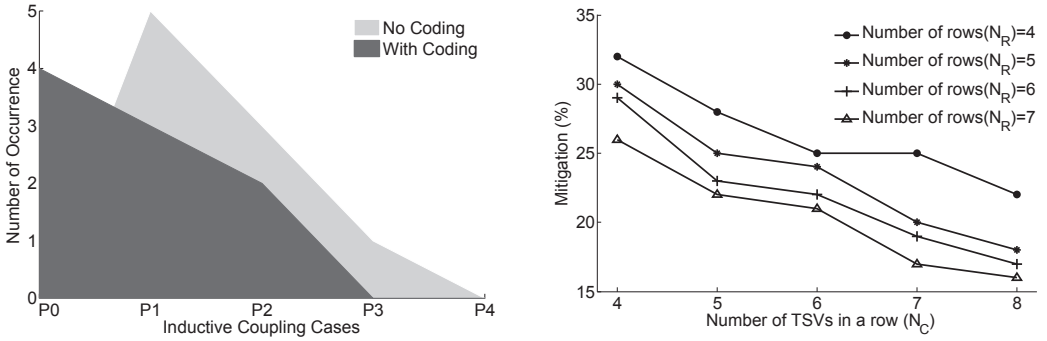


Fig. 6. Evaluation results for the given example

the corresponding element of the decision vector becomes 1 and the inverted values of the corresponding row of BMAT are transmitted through the TSV lines. Fig. 6 reports the the number of $P_{\alpha\beta}$ before and after employing the proposed coding for the presented example in Fig. 5. The number of $P_{\alpha\beta}$ with larger α values are replaced by $P_{\alpha\beta}$ with smaller α ones after applying the algorithm as shown in Fig. 6, resulting in lower chance of failure. The encoder/decoder is embedded in NI in order to implement the proposed algorithm. The encoder of proposed coding algorithm is implemented in Verilog and synthesized by Synopsys Design Compiler using 28nm TSMC library (1.05V, $25\,^{\circ}\mathrm{C}$) to report latency, power consumption, and area, as summarized in TABLE II. The total area overhead of the encoder component is $394\mu m^2$ with the latency of 23ps. The feasibility of the proposed coding method algorithm is confirmed by considering the gained coupled voltage mitigation and its negligible footprint and power consumption. Decoder unit is not implemented in this experiment since it is composed of a comparator and a mix of inverter gates. It is much lighter than encoder component in terms of area, power consumption, and latency. To evaluate the advantages of the proposed algorithm on the inductive TSV coupling, Monte Carlo simulations for 10000 iterations on a 4×8 2D mesh TSV configuration are examined. The 4×8 2D mesh TSV is chosen as our case study as flit sizes of 32-64 bits is common among NoC communities [18]. Fig. 7(a) compares the number of $P_{\alpha\beta}$ for all five possible α values before and after employing the proposed coding method in Monte Carlo simulation. The integration of $P_{\alpha\beta}$ are shifted to the left after using the proposed coding method; $P_{\alpha\beta}$ with larger α values are replaced by ones with smaller α values, resulting in reduction of failure chance of TSVs induced by inductive TSV coupling. It is of interest to analyze the variation of coupled voltage mitigation as TSV matrix dimensions grow. The result of this analysis, as demonstrated in Fig. 7(b), reports the effects of TSV configuration dimensions on the mitigation

TABLE II
Hardware Synthesis Results

Area			Power	
Sequential	**Combinational**	**Latency**	**Switch.**	**Leakage**
$121\mu m^2$	$272\mu m^2$	$23ps$	$15\mu W$	$646\mu W$



(a) (b)

Fig. 7. Evaluation results: (a) Average magnetic field values from simulation, (b) Rate of mitigation as the number of TSVs a row grows

improvement of the proposed coding algorithm. Each line in Fig. 7(b) shows coupled voltage mitigation for a fixed number of row (N_R) in a TSV matrix as the number of columns (N_C) grows. It is observed that increasing both (N_R) and (N_C) decreases mitigation improvement, however the negative effect of increasing N_C is more severe than the effect of increasing N_R for a fixed number of TSVs. For example for a given bundle of 24 TSVs, the mitigation percentage is reported 26% when a 4×6 array of TSVs is employed (N_R=4 and N_C=6). On the other hand, the mitigation percentage of 29% is achieved for a 6×4 array of TSVs (N_R=6 and N_C=4). The proposed algorithm is suitable for 3D NoC routers since the channel width of a typical NoC router is less than 64 bits [18]. As it is indicated in Fig. 7(b) for a 4×8 (N_R=4 and N_C=8) TSV configuration, the proposed coding achieves 23% coupled voltage mitigation by imposing 12.5% information overhead.

V. Conclusions and Future Work

A reliability analysis of inductive TSV-to-TSV coupling is presented in this article. Chance of failure for a victim TSV is also categorized in terms of its neighboring TSV aggressor currents, resulting in various inductively coupled voltages. The main goal of the proposed technique is to mitigate the effects of coupled voltage of TSVs on each other. The proposed algorithm monitors the data-bit pattern of consecutive flits to adjust current flow of active TSVs. A single bit overhead is employed for each row of TSV configuration as an information redundancy of the proposed algorithm. Future work might expand the proposed algorithm with other 3D application in which higher data bandwidth of TSVs are needed like 3D memory designs.

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