# Accurate System-level TSV-to-TSV Capacitive Coupling Fault Model for 3D-NoC

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## ABSTRACT

TSV-based 3D-NoC has been introduced as a viable solution for integrating more cores on a chip, while imposing smaller footprint area and better timing performance as compared to 2D-NoC. However, TSV-to-TSV coupling is increasingly impacting the reliability of 3D-NoCs due to large size of TSVs. Addressing this issue, various resilient approaches have been recently proposed. But they have been evaluated by uniform random distributions fault modelling, which results in 26%-99% inaccuracy. We propose a system-level TSV-to-TSV coupling fault model that models the capacitive coupling effect, considering thermal impact, with circuit-level accuracy. This model can be plugged into any system-level TSV-based 3D-NoC simulator. It is also capable of identifying faulty TSV bundles and evaluating the efficiency of alternative resilient TSV-based 3D-NoC designs at the system-level.

## Categories and Subject Descriptors

B.8 [**Hardware**]: Performance and Reliability

## General Terms

Reliability, Measurement

## Keywords

Fault modeling, TSV coupling, 3D NoC

## 1. INTRODUCTION

Today's process technology is expected to be scaled down to 7nm by 2020, while manufacturers will reach the fundamental physical limits of this trend. To keep technological progress in step with Moore's Law, researchers have suggested applying lower frequency many-core chips rather than a single-core with higher operational frequency. Network-on-Chip (NoC) has been proposed as a scalable and efficient on-chip interconnection among cores. In addition, employing Three-Dimensional (3D) integration instead of Two-Dimensional (2D) integration is the other trend to keep the traditional expected performance improvements [1]. The combination of 3D integration and NoC technologies provides a new horizon for on-chip interconnect design.

The 2D dies were initially connected by wire-bond, later by flip-chip, and recently by Through-Silicon Via (TSV). TSV-based 3D-NoCs are currently the most promising approach to deal with the limitation of 2D architectures for next generation fabrication technologies [2]. They offer higher bandwidth, smaller form factor, shorter wire length, lower power consumption, and better performance than traditional 2D-NoCs [3]. Although the impact of TSVs on Signal Integrity (SI) in 3D-NoCs has been investigated [4, 5], the reliability of TSVs is still an area of open research in the context of designing 3D stacked chip systems. TSV-to-TSV Capacitive Coupling (TTCC), which is the main focus of this article, is one of the major challenges for designing 3D multiple stacked ICs. TTCC occurs because of unexpected parasitic signals in 3D designs related to physical characteristics of TSVs. TTCC is responsible for two undesirable effects. First, it increases the path delay by slowing down transitions on signal-switching if neighbor TSVs perform opposite transitions. Second, the coupling noise may result in signal distortion by generating large glitches on a static signal when TSV's aggressor neighbors transition.

We present a fault model to quantify the impact of TTCC-induced faults at system-level with circuit-level accuracy. This model pinpoints fault-prone TSV links at runtime. This model is also able to report the efficiency of resilient TSV-based 3D-NoC designs for a given set of TSV characteristics, thermal impacts, and workloads.

The presented model can be utilized for application-specific designs by addressing the susceptible to failure TSVs. With these results a designer is able to employ fault-tolerant methods only where they are needed. For general purpose architectures, the presented fault model is able to figure out the effect of physical parameters of TSVs on timing requirement of the circuits. This model can be used to find the suitable physical parameters for a TSV to have reliable TSV links.

In more details the effect of TTCC on timing requirements of the 3D design are captured at circuit-level, and they will be applied in system-level simulations at runtime. This model takes advantage of both system-level and circuit-level modeling which results in shorter simulation time and more accurate experimental reports. Our proposed fault model is potentially useful for evaluating the reliability of 3D many-core applications in which TTCC may lead to failure. 3D memory and 3D-NoCs are two examples of these applications. In 3D memory applications [6], TTCC can corrupt

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the data or/and address bus. In on-chip network routers, data flit corruption may occur due to TTCC in which an Error-Correction Code (ECC) is needed for protection.
The major contributions of this article are:

- To elaborate TTCC effects on timing requirement of a circuit in order to present circuit-level fault library, which is discussed in Section 3. The proposed fault library is utilized at run-time in order to identify the TTCC effect automatically.

- To provide a system-level TTCC fault modeling framework for TSV-based 3D-NoCs, which is presented in Section 4. It can be integrated into any simulator (working with actual data flits) to detect and inject TTCC faults at runtime, and to evaluate resilient approaches.

- To present a case study, characterizing faults at runtime in a $4 \times 4 \times 4$ 3D-NoC architecture, which is explained in Section 5.

## 2. RELATED WORK

Based on an overview of the state-of-the-art fault-tolerant methods in the last decade [7], reliable NoCs have been proposed by presenting fault-tolerant routing algorithms [8, 9], reliable architecture [10], and error correction coding methods [11, 12]. Additionally, some research groups have suggested coding methods to alleviate parasitic capacitivenoises rather than removing them. Two coding approaches have been proposed to mitigate the undesirable effects of Inductive and capacitive TSV-to-TSV coupling effects [13, 14]. A power-efficient fault-tolerant method has been proposed in which the routers are capable of switching between error detection and error correction modes at run time [15].

Furthermore, some researchers have addressed the reliability evaluation of NoCs [16]. A classification of the potential physical faults in a baseline 3D NoC is discussed in [17]. This article also provides a reliability analysis for major sources of faults separately based on their Mean Time to Failure (MTTF). In addition, an analytical model for the coupling capacitance between pairs of TSVs is presented in [4]. However, all of these approaches are evaluated through the experiments in which the time and location of fault occurrences are chosen with uniform random distributions. In addition, based on our experiments, the evaluation of TTCC effects by injecting uniformly random faults is considered 26%-99% inaccurate in capturing time and locations of induced faults, as will be discussed in Section 5.2. In a similar work, a system-level process variation model has been proposed for 2D-NoC simulators [18], but it does not support TTCC effect in 3D-NoCs. On the other hand, although several crosstalk minimization techniques have been proposed in 2D designs [10, 19], they cannot be directly applied in 3D designs. This is because of the fact that the physical characteristics of 2D wires and TSVs are different. In addition 2D wires have at most two aggressors in the same layer of fabrication, while in 3D designs TSVs are surrounded by more aggressors [20]; making the crosstalk modeling and elimination more complicated for 3D-NoCs.

## 3. TTCC ELABORATION

The term TSV-to-TSV coupling refers to capacitive and inductive couplings between each pair of TSVs. Electric field results in capacitance coupling and magnetic field is a source of inductive coupling. This article targets the capacitive coupling effect that is more critical in lower range of operational frequencies (less than 5GHz) [21], which applies to NoC routers. In this section: first, a circuit-level TSV model for TTCC elaboration is discussed, although any other model can be replaced; second, a TTCC classification is presented; finally, the effect of TTCC on timing requirement of NoC router transmitter circuit is illustrated using realistic benchmarks.

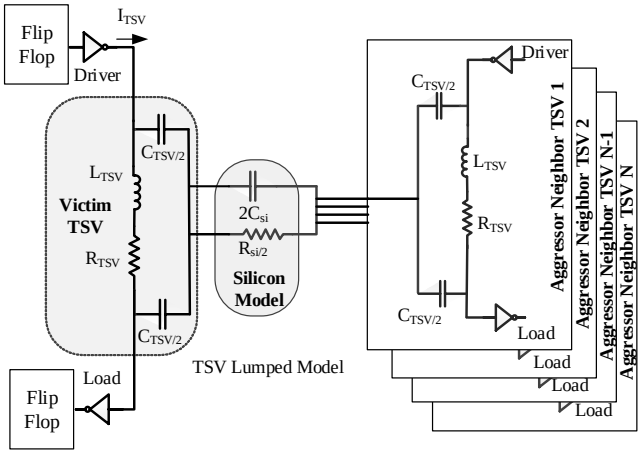



Figure 1: The block diagram of the induced capacitive coupling on each TSV based on physical parameters

### 3.1 TTCC Circuit-level Modeling

A framework consisting of multiple TSVs at circuit-level using Synopsys HSPICE is implemented in this experiment to study the sources of TTCC effect. Developing TSV simulation framework allows extracting the realistic accurate TTCC effect for different parameters. The coupled TSV structure is modeled as a lumped RLC circuit. We have utilized the lumped RLC circuit circuit-level model of TSVs presented in [22–24]. Figure 1 shows the used circuit-level in this article, in which $R_{TSV}$, $L_{TSV}$, $R_{si}$, $C_{si}$, and $C_{TSV}$ represent TSV resistance, TSV inductance, substrate resistance, substrate capacitance, and oxide capacitance, respectively. The value of the circuit elements are modeled using analytical equations based on the dimensions of the structure, such as oxide thickness, silicon substrate height, TSV radius, and TSV pitch and by material properties like dielectric constant and resistivity. These physical parameters are also extracted from ITRS reports [25]. The thermal impact is also considered in the TSV model using equations in [26]. Furthermore, since the parasitic capacitive effect of a diagonal neighboring TSV is less than 1/5 of an adjacent TSV neighbor [13], only the effect of adjacent TSV neighbors are examined in this experiment. However, our fault model can be expanded to support more TSVs as well.

For our analysis, a TSV is connected to the output of an inverter (driver) on one side and to the input of another inverter on the other side (load). These inverters are needed to record the propagation delay and its dependency to parasitic capacitivenoises. Two flip-flops, one before the driver inverter and one after the load inverter are inserted to capture the parasitic capacitive effects on timing requirements of the circuit. We compare the input data pattern with out-

$$\textbf{Data}_{i-1} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 1 \\ 0 & 1 & 0 \end{bmatrix} \quad \textbf{Data}_{i} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix}$$

$$\textbf{Current direction} = \begin{bmatrix} & \odot & \\ 2C & & 1C \\ \odot & \otimes & \odot \\ 2C & & 0C \\ & \otimes & \end{bmatrix} \quad \textbf{TTCC factors} = \begin{bmatrix} 2 & 4 & 1 \\ 4 & 5 & 1 \\ 2 & 2 & 1 \end{bmatrix}$$

Figure 2: Current and TTCC matrices in a $3 \times 3$ mesh of TSVs

put data pattern to catch the parasitic capacitive effects.

Predictive Technology Model (PTM) [27] FinFET transistor models are employed to implement inverters and flip-flops. Then a comprehensive set of simulations is performed on the developed TSV framework. The impact of operational frequency, temperature, technology, TSV radius, and TSV oxide thickness are investigated which is discussed in 3.2. SPICE model of TSVs are employed to examine the TTCC effect among a victim and its aggressor TSVs.

In this article we define path delay, as the propagation delay from the output of the driver inverter to the input of the load inverter after the rising edge of the clock. Nominal Path Delay (NPD) is the path delay when there is no TSV parasitic capacitive. Actual Path Delay (APD) may be longer than NPD due to the coupling effects generated by aggressor TSVs. Assuming the system clock is adjusted for a critical path of NPD, circuit timing requirement is violated when the APD exceeds the NPD. Timing Violation (TV) is defined as any additional delay over NPD (introduced by parasitic capacitive) normalized by clock period as presented in Equation 1:

$$TV = \frac{APD - NPD}{T_{clk}} = f_{clk}\,(APD - NPD) \qquad (1)$$

Running hundreds of simulations on the developed circuit model with different input data patterns, different TVs are reported; concluding that TTCC factors are data dependent. In other words, the TTCC effect on circuit timing is predictable by monitoring the data bit patterns fed into the TSVs, which is discussed in the following subsection.

## 3.2 TTCC Analysis

The TTCC classification is presented in this section is based on the severity of their parasitic capacitive factors. The parasitic capacitive value is a function of the charging and discharging of the victim TSV and its neighbors. Since between any two dies, the TSV drivers are all in one die and the loads are in the other die, the direction of the current in each TSV can specify the charging or discharging state. On the other hand, the current direction is data-

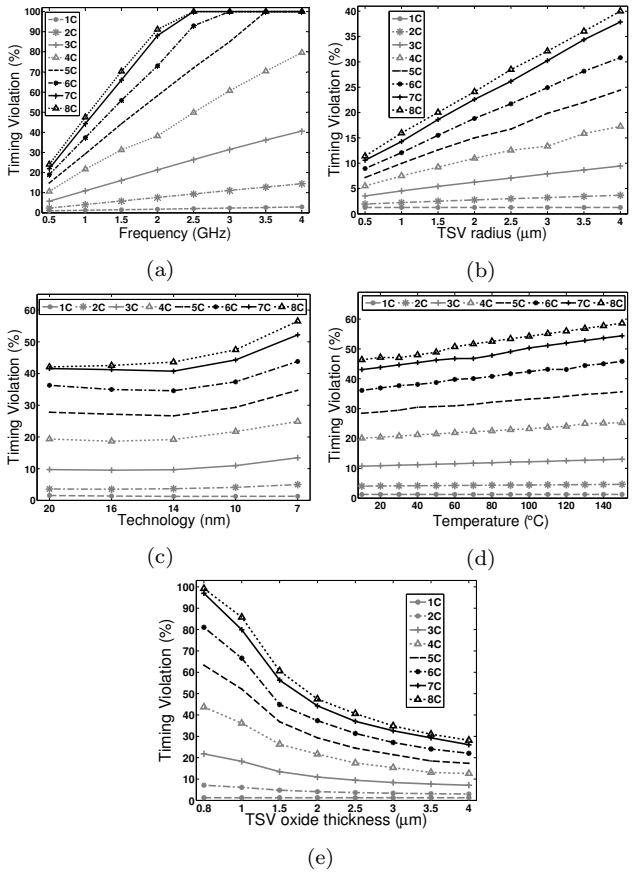



Figure 3: Characterizing TTCC against various parameters

dependent. Therefore, TTCC depends on the data pattern. This explanation confirms our previous observation in which TTCC factors are data dependent. However, both the previous ($Data_{i-1}$) and current ($Data_i$) data bit value of a TSV's driver are needed in order to identify the current direction of each TSV. According to current direction detection process of a TSV in [14], there are three possible current directions for TSVs: Upward ($\otimes$), Downward ($\odot$), and No-current ($\bigcirc$). In the rest of this article, a TSV with No-current is called an inactive TSV, while a TSV with Downward/Upward current is called an active TSV.

With these assumptions, the parasitic capacitive between a pair of TSVs is represented by 0C (if they both have the same current direction), 1C (if one of them is inactive and the other is active), 2C (if they have reverse current direction).

The total capacitive coupling voltage on the victim TSV is equal to the sum of voltages coupled by each aggressor on the victim TSV. If an upward current is represented with

Table 1: TTCC factor categorization

| Types | 0C | 1C | 2C | 3C | 4C | 5C | 6C | 7C | 8C |
|---|---|---|---|---|---|---|---|---|---|
| Sample pattern | $\begin{matrix} & \odot & \\ \odot & \odot & \odot \\ & \odot & \end{matrix}$ | $\begin{matrix} & \odot & \\ \odot & \odot & \odot \\ & \bigcirc & \end{matrix}$ | $\begin{matrix} & \odot & \\ \odot & \odot & \odot \\ & \otimes & \end{matrix}$ | $\begin{matrix} & \odot & \\ \odot & \odot & \bigcirc \\ & \otimes & \end{matrix}$ | $\begin{matrix} & \odot & \\ \odot & \odot & \otimes \\ & \otimes & \end{matrix}$ | $\begin{matrix} & \bigcirc & \\ \odot & \odot & \otimes \\ & \otimes & \end{matrix}$ | $\begin{matrix} & \otimes & \\ \odot & \odot & \otimes \\ & \otimes & \end{matrix}$ | $\begin{matrix} & \otimes & \\ \bigcirc & \odot & \otimes \\ & \otimes & \end{matrix}$ | $\begin{matrix} & \otimes & \\ \otimes & \odot & \otimes \\ & \otimes & \end{matrix}$ |
| Occurrence frequency | 3 | 16 | 44 | 64 | 54 | 32 | 20 | 8 | 2 |
| Occurrence probability | 0.01 | 0.07 | 0.18 | 0.26 | 0.22 | 0.13 | 0.08 | 0.03 | 0.01 |

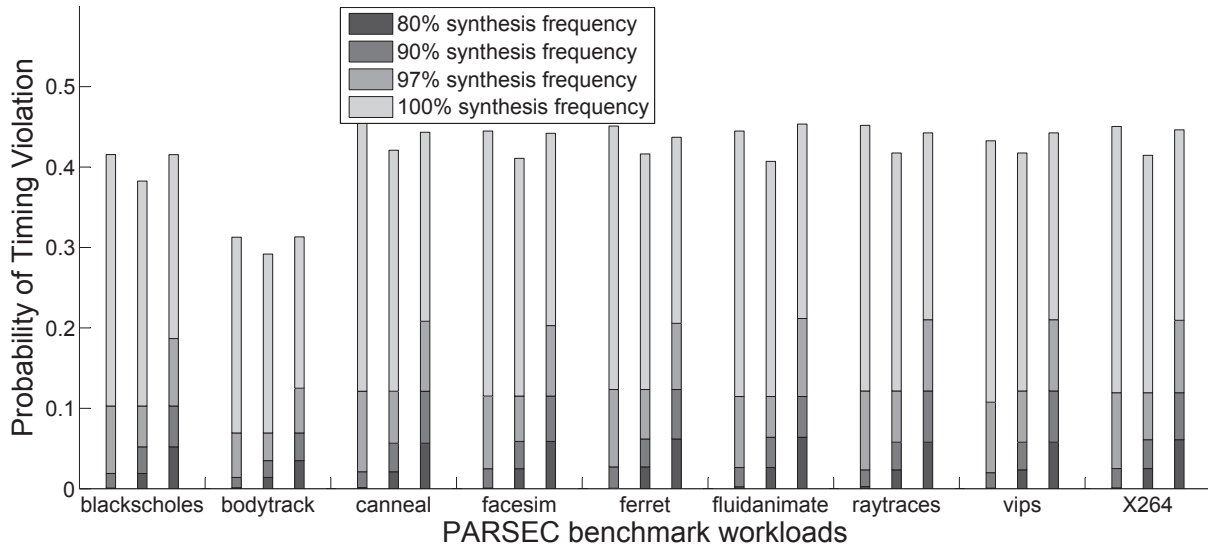



Figure 4: Probability of TV in PARSEC benchmark workloads under different conditions (Table 2)

+1, a downward current with -1 and no-current with 0, total TTCC can be quantified by Equation 2:

$$TTCC_{tot} = \sum_{i=1}^{N} |d_{vic} - d_{agg_i}| \quad (2)$$

where $TTCC_{tot}$ is the total parasitic capacitive factor for each TSV, $N$ represents the number of adjacent aggressors for a victim TSV, and $d$ is the current direction for the corresponding TSV. The $TTCC_{tot}$ factors are used for categorizing parasitic capacitive types in this article as shown in Table 1. Figure 2 shows an example of current matrix generation and consequently TTCC factors on the victim TSV (the middle one), caused by its adjacent neighbors in a mesh of $3 \times 3$ TSVs. The $TTCC_{tot}$ value on the victim TSV for the given example in Figure 2 is equal to 5C.

There are $3^5 = 243$ possible TSV arrangements for 5 TSVs, one victim and four adjacent TSVs, with 3 possible current directions. In each of these arrangements the $TTCC_{tot}$ factor will be in range of 0C to 8C as discussed in Equation 2.

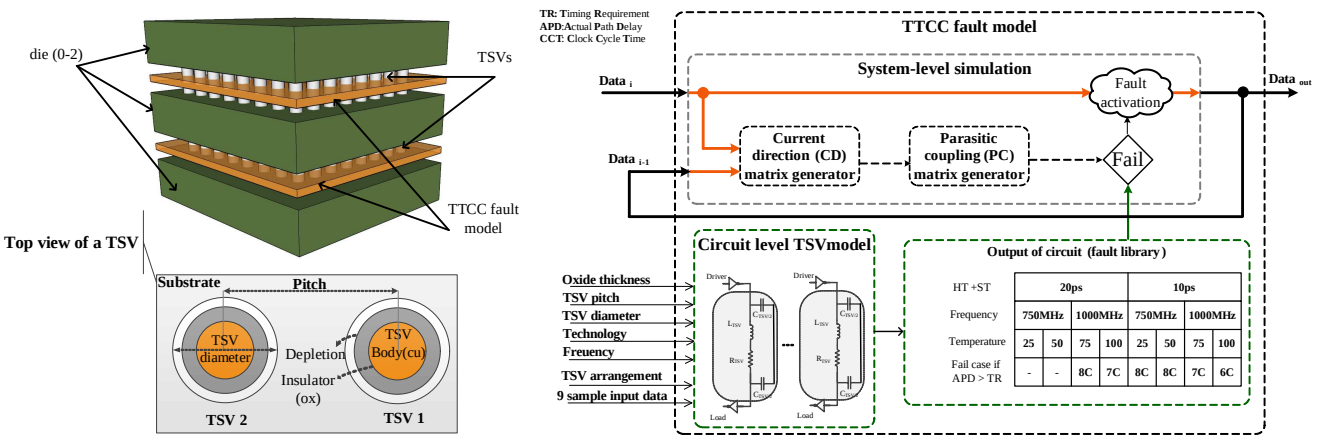
The frequency and probability of occurrence of each of the $TTCC_{tot}$ factors are summarized in Table 1. For further illustration, a sample pattern resulting in the corresponding parasitic capacitive type is also shown in this table. The maximum capacitive coupling voltage on a victim TSV in this representation is equal to 8C if the middle TSV has reverse current direction as compared to all of its neighbors, shown in the right most column of Table 1.

In addition, these capacitive coupling factors may disrupt timing requirement of 3D-NoC depending on the operational frequency and TSV physical parameters. We have characterized the effect of TTCC for each of parasitic capacitive types presented in Table 1 using our circuit-level model. This characterization for a range of operational frequency and different TSV parameters is elaborated in Figure 3. In Figure 3a, increasing clock frequency does not have tangible effect on the TTCC severity, but TV is increasing linearly for larger operational frequencies. This is because timing requirement gets tight in higher frequencies. For TSVs with larger radius and the same pitch value, $C_{si}$ will increase and therefore more capacitive coupling is observed, as shown in Figure 3b. As the technology advances, the loading voltage of the flip-flop over the TSV decreases, resulting in larger coupled voltage on the TSV (shown in Figure 3c). The permittivity of the silicon rises as a weak linear function of temperature [26], which increases $C_{si}$ and consequently the TV, as depicted in Figure 3d. Finally, as shown in Figure 3e, thicker oxide provides better isolation and reduces the value of $C_{TSV}$, producing less capacitive coupling and consequently less TV.

## 3.3 TTCC Effect on TV

Having analyzed and modeled the TTCC, we have evaluated its effect on realistic data traffic using PARSEC benchmark. This realistic data benchmark is transferred through the circuit-level model of 64 TSVs for various configurations. The TV values on the receiver side of each TSV is recorded. A configuration is a set of physical parameters including TSV radius, length, pitch, oxide thickness, and process technology, operating frequency, and temperature. The configuration values are selected in a way to cover different TTCC effects. Figure 4 shows the probability of TV for PARSEC benchmark workloads for three different TSV configurations (presented in Table 2). Each group of three bars in this figure from left to right refer to configurations A, B, and C in Table 2.

In addition, the TV probabilities are reported for different percentage of maximum synthesis frequencies. The results show that, the percentage of TV for lower synthesis frequency drops down for all workloads, however, an average of 40% TV at 100% synthesis frequency still confirms the importance of TTCC analysis for TSV-based 3D-NoC architectures. Furthermore, the result of Figure 4 shows how TTCC limits the maximum operational frequency of 3D NoCs. The reason is that the propagation delay of TSVs are extended as an effect of TTCC. In other words, the circuit is able to handle more percentage of TV with lower operational frequency.




(a) Fault model location in IC simulator

(b) Fault model

Figure 5: Fault Model usage demonstration in 3D-NoC

Table 2: Different configuration of TSV arrays

| Configuration | A | B | C |
|---|---|---|---|
| radius $\mu m$ | 3 | 3 | 2 |
| length $nm$ | 15 | 20 | 25 |
| pitch $\mu m$ | 9 | 9 | 6 |
| $T_{ox}$ $\mu m$ | 3 | 2.5 | 1 |
| Technology $nm$ | 20 | 16 | 10 |
| Max Freq. $GHz$ | 1 | 1 | 1 |
| Temperature $^{\circ}C$ | 50 | 75 | 100 |

## 4. TSV COUPLING FAULT MODEL

Circuit-level simulation takes much longer than system-level simulation. A fault model is proposed in this paper that that can accurately assess TTCC faults. This approach considers the effects of circuit-level representation of TTCC for a system-level platform to reduce simulation time while maintaining accuracy. This operation is performed at run-time by monitoring the data signals that are being transmitted through TSVs in order to identify where and when potential faulty TSVs occurred. Next these candidate faulty TSVs are triggered with the observed effect at the circuit-level of TTCC fault.

Figure 5 shows the 3D-NoC framework and the proposed TTCC fault model. The fault model is envisioned to be employed as an intermediate component among TSVs connecting routers in different dies, as shown in Figure 5a. This fault model does not affect the functionality of 3D-NoC; it only decides the time and location of fault activation through the TSVs based on data input patterns and the provided fault library at the circuit level. Figure 5b depicts the functionality of our proposed fault model in details. The input parameters of our circuit-level model are TSV arrangement configuration (Number of rows and columns) connected to 3D-NoC, operating frequency, process technology, silicon oxide thickness, TSV-to-TSV pitch, TSV length, and TSV diameter. The output of this model is a table, which shows the corresponding parasitic capacitive factors violating the timing requirements for each configuration. An example of the fault library table is shown in Figure 5b. This output is used as a fault library in our system-level simulation, in which the parasitic capacitive factors are extracted by comparing the transmitted ($Data_{i-1}$) and ready to transmit ($Data_i$) data bits through TSVs. With this configuration the TTCC fault model decides intelligently and accurately when and where a TTCC fault should be activated. The steps of this methodology are as follows:

- **Step.0 Configuration and Setup:** Prior to instantiating and utilizing the devised TTCC fault model, first it needs to be configured and setup. In this phase, input parameters of the model such as the TSV length, TSV diameter, TSV pitch, oxide thickness of TSVs, process technology, frequency, and temperature are specified. Frequency and temperature parameters are defined as a range with a specific granularity to support dynamic changes at run-time. The other inputs of the circuit-level model is all the possible data inputs resulting in 9 parasitic capacitive factors from 0C to 8C.

- **Step.1 Capturing transferred data:** In this step, the data bits transferring through TSV links (Up/Down port) are captured as the input of fault model at run-time. These captured data bits are adjusted if the fault activation condition is met.

- **Step.2 Data analysis to determine the TSV current directions:** At this step, the current directions of all TSVs are identified. The previous ($Data_{i-1}$) and current ($Data_i$) data-bit values of a TSV's driver are profiled and compared in order to recognize the current direction of each TSV. This process is done with the same approach as discussed in [14]. The output of this stage is stored as Current Direction (CD) matrix.

- **Step.3 Determine the induced capacitive coupling case for each TSV:** Looking at the current direction of each TSV and its adjacent neighbors, in this step an appropriate capacitive case is assigned per TSV. Now the fault library generated at pre-runtime is used to look up the timing delay associated for the corresponding case and is recorded as Parasitic Coupling (PC) matrix.

- **Step.4 Map circuit-level faults to system level delay fault/failure for each TSV:** Considering the timing requirement parameter of the destination receiver flip-flop

Table 3: System configuration parameters

| Parameter | Value |
|---|---|
| Topology | 3D fully connected Mesh |
| Network Size | (4x4x4) 64 Routers |
| Flit Size | 32 bits |
| Buffer Depth | 8, 16-bit entries per port |
| Switching Scheme | Wormhole |
| Routing Algorithm | Dimension Ordered Routing |
| Simulator | THENoC [28] |

(input buffer of receiver router), at this point, using PC matrix, the decision for faulty TSVs is made and an appropriate fault is applied to the detected faulty TSVs. If the reported timing delay associated with the capacitive case violates the timing requirement of the receiver logic, then the data bit is assumed faulty. The fault type, depending on the specified delay tolerance for the circuit, can be either a *"delay fault"* or a *"glitch fault"*. However, if the specified timing requirement of flip-flop tolerates the undesirable propagation delay because of TTCC, then this fault will not have any impact and it is ignored in the model. Now the data is ready to be forwarded towards destination. Also a copy of last transmitted data (flit) is maintained for subsequent current direction determination.

# 5. CASE STUDY: DIAGNOSING TSV COUPLING AT RUNTIME IN 3D-NoC

A case study is presented in this section to show the capability of the proposed TTCC fault model at the system-level. First, the simulation infrastructure details are discussed. Then, the accuracy of our fault model is compared. This is followed by reporting the number of TTCC faults due to TV in each data transition under PARSEC benchmarks , and finally, a resilient solution with the proposed fault model is investigated. Each of these capabilities are important for 3D-NoC designers to assess their design's sensitivity against TTCC under various TSV physical parameters and operating conditions accurately.

## 5.1 Simulation Configuration

A cycle-accurate simulation, on the 64-node 3D mesh NoC (the simulation parameters are shown in Table 3) is performed. Our proposed TTCC fault model is implemented at the system-level in C. In the developed 3D-NoC, TSV bundles between each router in different layer are connected through the proposed coupling fault model. This fault model locates and triggers the parasitic capacitive for the specific configuration of TSVs with the given physical parameters, as elaborated in Section 4. Prior to running the simulation, each configuration is run in HSPICE and the result is passed as a static configuration library to the C model. Using the information provided by HSPICE (fail cases) and the CD matrix, our fault model detects the coupling fault and triggers it accordingly on-the-fly. The fault model operation is detailed in Section 4 and is illustrated in Figure 5b.

## 5.2 Fault model accuracy

In order to demonstrate the accuracy of our fault model, a comparison is made with a crosstalk fault model [18]. These faults are activated with the uniform random distribution. The comparison shows that the accuracy of conventional

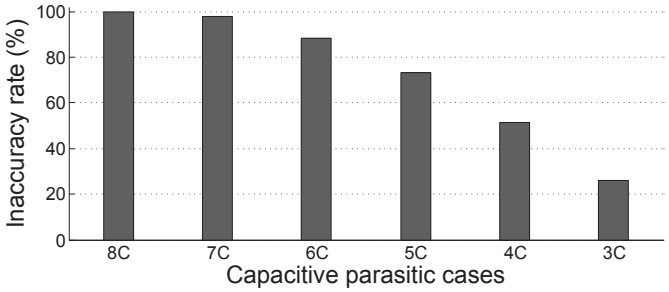



Figure 6: Inaccuracy introduced by random fault models

fault model for TSVs is substantially inaccurate.

First, a 3D-NoC simulation with the TTCC fault model using random traffic is performed and the number of fault occurrences for a TSV bundle is calculated. Then, using conventional fault model, the 3D-NoC simulation is run for 10000 iterations while in each experiment, faults are injected randomly across the TSV bundles to measure the reliability analysis inaccuracy. These simulations are repeated with different configurations, where a failing case is the result of parasitic capacitive with a minimum value of 8C, 7C, 6C, 5C, 4C, or 3C. Considering that each capacitive case has a different probability of occurrence, as depicted in Table 1, these probabilities are considered in random fault injection simulations. For example, if 6C parasitic coupling results in failure based on our circuit-level modeling in a given configuration, the failure probability of a TSV in random simulation will be equal to the occurrence probability of 8C, 7C, or 6C which is 10/81. For a fair comparison, we also extracted the occurrence probability of capacitive coupling higher than 4C and 6C for TSVs on the corner and boundaries in a TSV bundle.

Figure 6 shows the inaccuracy introduced by random fault model distribution for different TSV configurations (leading to different failing cases). The inaccuracy of 0% corresponds to the distribution matching our model's probability of occurrence, while 100% inaccuracy implies that the random distribution does not predict the corresponding fault type occurrence. It is observed that randomly distributed faults across the $8 \times 8$ TSV bundle introduces almost 99% inaccuracy for a given TSV specification leading to 8C capacitive coupling case. However, inaccuracy percentages decrease as the factor of failing cases of parasitic capacitive reduces. The reason is that the occurrence probability of parasitic capacitive with smaller values are higher than the ones with larger factors. Consequently, the percentage of inaccuracy decreases for smaller parasitic capacitive causing failure. However, even with these considerations the 26% inaccuracy for 3C parasitic capacitive value is still reported.

## 5.3 TTCC Fault Characterization

In order to demonstrate the effects of network traffic on TTCC fault, the PARSEC benchmark traces were collected using GEM5, and then injected them into our $4 \times 4 \times 4$ 3D-NoC simulator which its specifications is summarized in Table 3. Figure 7 shows the ratio of TV occurrence over total number of data transactions in vertical direction for three different configuration (described in Figure 4) at 90% synthesis frequency. For *Configuration C*, an average of 18% TV is observed because of running at higher temperature

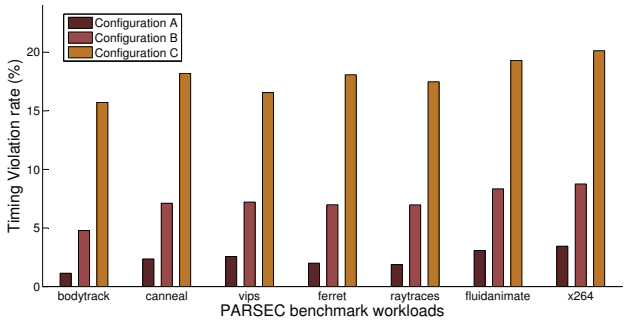



Figure 7: Fault Model usage demonstration in 3D-NoC running PARSEC benchmark under different conditions (Table 2)

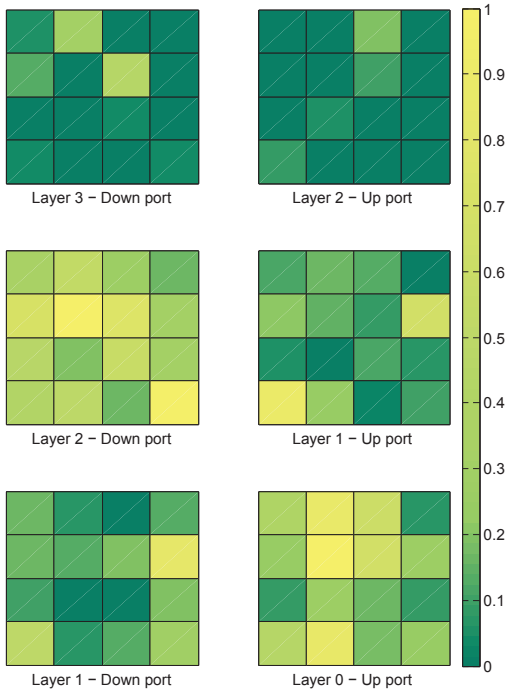



Figure 8: Fault Density Map

and low TSV oxide thickness which exasperate the TTCC. As the configuration parameter values get relaxed, the TV due to TTCC also decreases accordingly.

TTCC fault density map for the $4 \times 4 \times 4$ simulated network with *Canneal* workload traffic is depicted in Figure 8. This figure illustrates $4 \times 4$ NoC routers of a specific layer sending data to their lower/upper layer routers (*Down port*/*Up port*). The values are normalized to the maximum number of TV in entire 3D-NoC. The layer 0 down port and layer 3 up port are not shown since they do not exist. With this map designers can have better knowledge of placing their resiliency methods for an specific application. It can be seen that the data transactions from *layer 2* downward *layer 1* cause a large number of TTCC faults.

## 5.4 TTCC Fault Characterization with Resilient Approach

In order to show the advantage of our coupling fault model for fault-tolerant NoC designers, we model a simple inversion

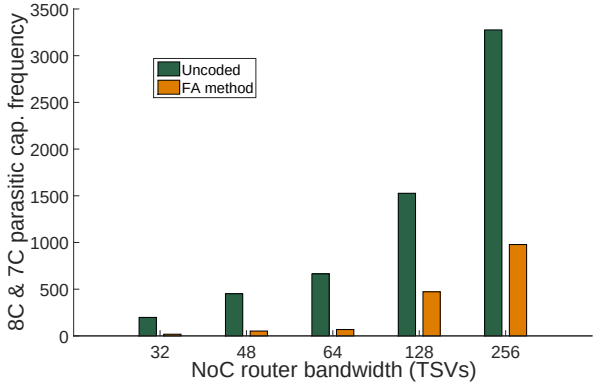



Figure 9: Number of 7C/8C for random data bit patterns in small mesh of TSVs

technique to avoid the most aggressive capacitive coupling cases, 7C and 8C, in each NoC router. State-of-the-art research in 3D-NoC design has explored various TTCC fault mitigation approaches to protect fault-prone TSVs.

The basic idea of this method is to modify the configuration of sequential data bits feeding TSVs by a light encoding approach. The inversion operation is chosen as a simple but light and efficient practical coding method in this experiment in order to keep the overhead low, while mitigating parasitic capacitive factors. This is a popular Fault Avoidance (FA) approach in order to mitigate both inductive and capacitive coupling effects in 3D-NoC designs [14, 20]. In this method two consecutive data bit values which are transferred through a single TSV link are examined to report the generated parasitic capacitive factors in a mesh of TSVs of NoC router as discussed in Section 3.2. Each row of 2D array of TSVs including 8C or 7C parasitic capacitive factors is nominated for the data encoding process. By encoding the ready to transmit data bits, 8C parasitic capacitance will be 4C and 7C parasitic capacitance will be 1C or 2C.

Figure 9 shows the number of 8C and 7C parasitic capacitance fault frequency before and after applying FA coding method between two vertically adjacent routers in a 3D NoC. We repeat the experiment for different router port bandwidth, ranging from 32 to 256, using uniform random synthetic traffic. The observation results of our proposed TTCC fault model after applying FA technique, results in a considerable reduction in the number of coupling faults.

# 6. CONCLUSIONS

A TSV-to-TSV capacitive coupling fault model was presented which can be easily deployed in system-level 3D-NoC simulators to detect the TSV-to-TSV capacitive coupling fault at runtime as part of any dynamic fault injection process. Our model facilitates the exploration of resilient TSV-based 3D-NoCs and help researchers accurately evaluate their 3D systems when dealing with TSV capacitive coupling. The core of our fault model is implemented at the circuit-level to collect accurate timing violations for each of parasitic capacitive cases, although the interface is implemented at the system-level. This model is useful for both application-specific and general purpose designs. For application specific designs our fault models reports the susceptible to failure TSVs. For general purpose applications it can

be applied to optimize the physical parameters of TSV to reduce the propagation delay of TSVs caused by TTCC.

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