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# A high level power model for Network-on-Chip (NoC) router

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ABSTRACT

This paper presents a high level power estimation methodology for a Network-on-Chip (NoC) router, that is capable of providing cycle accurate power profile to enable power exploration at system level. Our power macro model is based on the number of flits passing through a router as the unit of abstraction. Experimental results show that our power macro model incurs less than 5% average absolute cycle error compared to gate level analysis. The high level power macro model allows network power to be readily incorporated into simulation infrastructures, providing a fast and cycle accurate power profile, to enable power optimization such as power-aware compiler, core mapping, and scheduling techniques for CMP. As a case study, we demonstrate the use of our model for evaluating the effect of different core mappings using SPLASH-2 benchmark showing the utility of our power macro model.



## 1. Introduction

Technology scaling has enabled designers to integrate a large number of processors onto a single chip, realizing chip multi-processor (CMP). Thus, technology for high performance computing for CMP has been gaining the attention of the high performance computing community in the past few years. As the demand for network bandwidth increases for CMP, on-chip interconnection network, the idea of Network-on-Chip (NoC), has shown great promise in terms of performance, power, and scalability in SoC design [1].

Although today's processors are much faster and far more versatile than their predecessors using high-speed operation and parallelism, they also consume a lot of power. Moreover, an interconnection network dissipates a significant fraction of the total system power budget. For instance, the MIT Raw on-chip network consumes 36% of the total chip power and Alpha 21364 microprocessor dissipates 20% of total power in interconnection network [2]. Therefore, interconnection network must be designed to be power-aware. It is desirable to get detailed trade offs in power and performance early in the design flow, preferably at the system level. However, there is limited tool support available for power analysis of an interconnection network.

Power models are classified based on different levels of abstraction. The lowest level of abstraction is gate level which represents the model at transistor level and is more accurate than any of the higher levels. These models are extremely time consuming and intractable as far as power profile for complicated multi-processors are concerned. The next level in the abstraction is the register transfer level, which considers the transfer of data at register and wire level. The highest level of abstraction is the system level which emulates the functionalities performed without going into the hardware details of components. This level is less accurate but also requires less simulation time.

In this paper, we propose a framework for router power analysis that uses the number of flits passing through a router as the unit of abstraction in order to speed up of network simulation because the detailed modeling at the low level abstraction

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can further exacerbate the complexity of simulator. When validated against gate level simulation, our power model derives power profiles that match closely with that of gate level analysis. The high level power macro model allows network power to be readily incorporated into simulation infrastructures, providing a fast and cycle accurate power profile, to enable power optimization such as power-aware compiler, core mapping, and scheduling techniques for CMP. By evaluating the effect of different core mappings using SPLASH-2 [3] benchmark, how power analysis can facilitate power optimization of tiled CMP is demonstrated.

The rest of this paper is organized as follows. In Section 2, we discuss prior related works and address the novel contributions of our approach. Networked Processor Array (NePA) architecture is introduced in Section 3. Section 4 presents the details of our power estimation framework and Section 5 shows the validation of our model against gate level power analysis with synthetic traffic patterns. The case studies in application mapping on mesh network outline the potential ways of leveraging our power macro model in Section 6. Finally, Section 7 concludes the paper.

## 2. Related works

One way to model power consumption of an NoC is to derive detailed capacitance equations for various router and link components, assuming specific circuit design for each component. These equations are then plugged into a cycle accurate simulator so that actual network activity triggers specific capacitance calculations and derives dynamic power estimates. The capacitance for each network component is derived based on architectural parameters. The other approach is to evaluate the energy and power consumption of each component by using gate level simulation with technology libraries. There have been several power estimation approaches for network components in NoC. Patel et al. [4] first noted the need to consider power constraints in interconnection network design, and proposed an analytical power model of switch and link. Wang et al. [5] presented the architectural-level parameterized power model named Orion by combining parameterized capacitance equations and switching activity estimations for network components. These analytical models are based on evaluation of switching capacitance and estimate dynamic power consumption. Chen and Peh [6] extended the Orion by adding the leakage power model, which was based on empirical characterization of some frequently used circuit components. Ye et al. [7] analyzed the power consumption of switch fabric in network routers and proposed the bit-energy model to estimate the power consumption. However, the models are tightly coupled with circuit implementations. As such, these models cannot be migrated to different technology libraries without a large amount of re-modeling. Moreover, low level of abstraction (i.e. gate and device level) and the extremely slow simulation make it definitely unsuitable to face with system level SW/HW exploration task.

Statistical approach based on multiple linear regression analysis was adopted to generate power estimation. Bona et al. automated the extraction of a power model for the STBus, a high performance industrial communication architecture supporting shared buses as well as crossbars, based on regression technique [8] and presented an effective methodology to minimize the Design of Experiments (DoE) in [9]. However, a packet switched router components are not included in the STBus. Palermo et al. [10] proposed automatic generation of an analytical power model of network elements based on design space parameters and the traffic information derived from simulation. Wolkotte et al. [11] derived energy models for packet switched and circuit switched routers by calculating the average energy per bit to traverse on single router based on possible scenarios empirically. They insisted that the power consumption of a single router depends on four parameters: (1) the average load of every data stream; (2) the amount of bit-flips in the data stream; (3) the number of concurrent data streams; and (4) the amount of control overhead in a router. Penolazzi et al. [12] presented an empirical formulation in order to estimate the power consumption of the *Nostrum* NoC. They chose reference power with static input, number of total switching bits, number of static logic one bits, and total number of static bits as parameters for the analysis. The accuracy of their model demonstrated the average difference with respect to gate level simulation to be about 5%. Meloni et al. [13] presented power model for *xPipes* switch [14] with average error of 5%, but it provides a high level dependence on traffic variables instead of a cycle-by-cycle one. Chan et al. [15] attempted to build a cycle accurate power model of a target router instance where the absolute average error is 5% and average absolute cycle error is less than 20%.

In order to speed up the power simulation, Eisley and Peh [16] approximated NoC power consumption based on link utilization as the unit of abstraction. However, the model is not cycle accurate. Xi and Zhong [17] presented a transaction-level power model for switch and link in SystemC, providing both temporal and spatial power profile but the accuracy of the model was not discussed.

The novel contributions of our works are:

(1) a high level of abstraction by using the number of flits passing through a router as the unit of abstraction offers the system designers not only fast simulation speed, but also easy programming model suitable to system level design exploration since it does not need to consider the detailed gate level behavior of a router;
(2) the use of state information of FSM in a router which is employed to reserve channel during the entire packet forwarding for wormhole flow control enhances the accuracy of the power macro model;
(3) a cycle accurate power macro model provides temporal and spatial power profiling with less than 5% average absolute cycle error and less than 1.5% average error against that of gate level analysis; and
(4) a semi-automated extraction of the power macro model based on regression analysis can be easily migrated to different technology libraries.

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## 3. NePA: Networked Processor Array

### 3.1. Overview

NePA is a scalable, flexible, and reconfigurable multi-processor platform which is a two-dimensional processor array with mesh topology (see Fig. 1). This reconfigurable multi-processor platform includes multiple programmable processors, memory modules, and several application specific IPs which are required as part of the system specification. By virtue of scalability of NoC, the number of connected processors or IPs is not fixed in this platform. A scalable multi-processor architecture allows parallel processing for several applications on NePA. Current NePA platform includes a complete multi-core NoC simulator written in SystemC and a synthesizable RTL model written in Verilog HDL where adaptive routers, NI, and processors (compact version of OpenRISC) are integrated. The compact OpenRISC [18] is connected with our optimized router [19] through the NI [20]. NePA supports programmability and DSP related software are implemented and tested to show its potential as an embedded multi-core solution. Each router communicates with its four neighbors, providing communication channels for integrated PE.

### 3.2. Adaptive router architecture

Fig. 2 shows the block diagram of an $n \times m$ network router architecture [19]. A network router consists of four parts: (1) the header parsing unit (HPU) for each incoming port, (2) the finite state machine (FSM) for each outgoing port, (3) the arbitration unit (arbiter), and (4) the switch fabrics (multiplexer). The HPU inspects the head flit and generates signals for the arbiter. The arbiter completes the path decision based on arbitration algorithm. The FSM for each outgoing port supports flow control and delivers flits to their destination ports. The multiplexer unit connects the incoming ports to the outgoing ports.

The packet forwarding task follows a simple, adaptive routing, that uses a wormhole switching technique with a deadlock- and livelock-free algorithm for 2D-mesh topology. The packet structure, shown in Fig. 3, includes two major fields. One is the destination address $(\Delta x, \Delta y)$ field to indicate the destination node in the head flit. The address of the destination node is represented by the relative distance of horizontal and vertical direction, thus it is updated after each transition. The second field consists of a tag and the number of data to be exchanged. The body flits deliver the data to the destination node.

For the outgoing channel allocation, the router applies a fixed priority scheme to reduce the complexity of the router. The possible incoming channels have a descending order of priority in a clock-wise direction for each outgoing channel. Similarly, for the outgoing channels, a clock-wise order of priority is given. The incoming packets from node and output channel to node have the lowest priority in each priority group.

The routing algorithm was compared with *DOR* [21], *ROMM* [22], and *O1TURN* [23] algorithms in [24]. The router models were written in SystemC and simulations were executed with different traffic patterns. The routing algorithm showed same or better performance for all traffic patterns in $4 \times 4$ mesh topology. For the traffic patterns, it sustained highest offered traffic amount with the lowest average latency. Though it had slightly lower performance than *O1TURN* at $8 \times 8$ mesh topology, it still showed competitive performance. However, at the given amount of offered traffic before saturation point, it demonstrated the best performance with respect to the average latency.

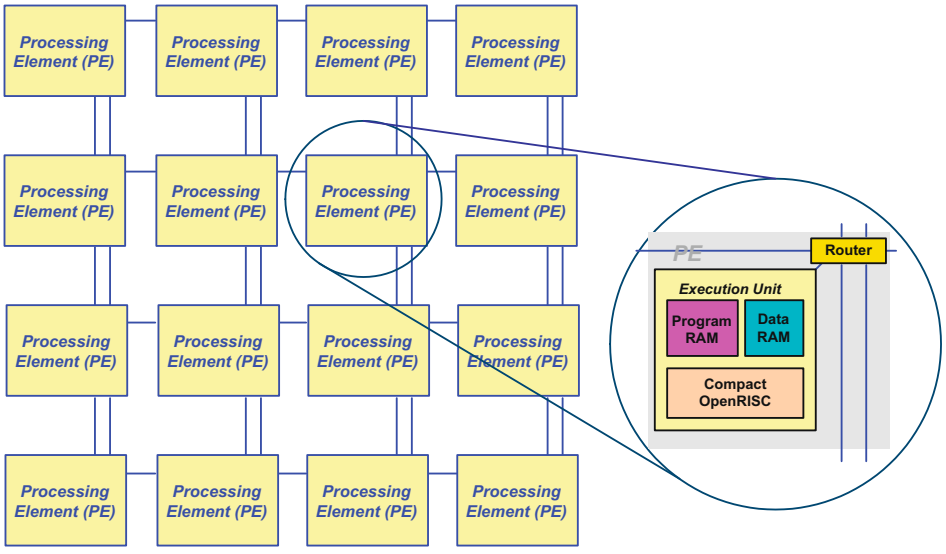


**Fig. 1.** Homogeneous NePA platform.

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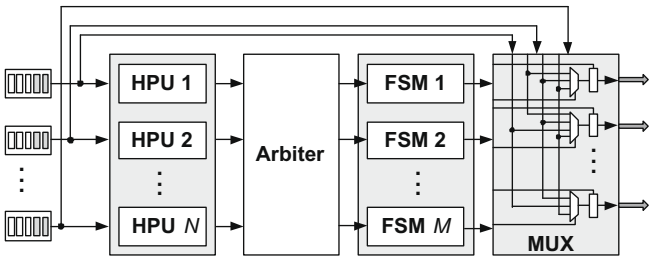


**Fig. 2.** Block diagram of a network router.

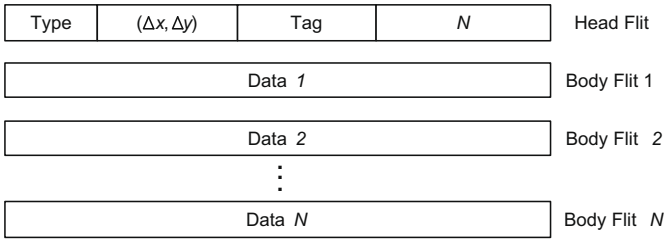


**Fig. 3.** Message structure.

The power consumed by an intermediate buffer depends largely on the amount of buffering and the architecture of buffer (memory or register based). The main purpose of our research is to determine the amount of power consumed in a router. In the following sections, we will analyze the power consumption on a router and formulate the power macro model.

## 4. Power modeling of a router

### 4.1. Power macro model

We create a power macro model for a single router, which consists of variables, that have a strong correlation to power consumption, and regression coefficients, that reflect the contributions of the variables for power consumption as follow:

$$\widehat{P} = \alpha_0 + A \cdot \Psi \tag{1}$$

where $A = [\alpha_1 \alpha_2 \ldots \alpha_k]$ and $\Psi = [\psi_1 \psi_2 \ldots \psi_k]^T$. $\alpha_0$ is the power term which is independent on the variables, and $A$ is the regression coefficients for the variables $\Psi$.

Power macro modeling is to find out the regression coefficients for the variables, which provide the minimum mean square error.

### 4.2. Methodology

The methodology used to create a power model for our work is illustrated in Fig. 4. We start with a packet synthesizer which generates traffic patterns that exercise the router under different conditions (Step 1). The RTL description is synthesized to the gate level net-list with Synopsys Design Compiler™ [25] using technology library (Step 2). As a part of this step, physical information such as RC parasitic value files (SPEF), standard delay format (SDF) and design constraints file (SDC), are also generated to be used for gate level power analysis. The gate level simulation extracts the switching information of the variables $\Psi$ for modeling and dumps a value change dump (VCD) file for the power analysis (Step 3). Power analysis with Synopsys PrimeTime™ PX tool [25] creates nano second detailed power waveform using switching and physical information (Step 4). In order to develop cycle accurate model, the extracted waveform is modified to a cycle level granularity power waveform.

#### 4.2.1. Hierarchical power modeling

A hierarchical power characterization model for custom IP cores was introduced enabling a trade-off among power estimation accuracy, modeling effort and estimation speed [26]. Upper levels represent coarser grained power models, while lower levels represent more accurate models with greater detail.

For the hierarchical power model of a router (Step 5), the power consumption of a router was analyzed at 100 MHz using 90 nm technology to estimate the power dissipated by various parts of the router. Maximum power is consumed by the FSM of outgoing ports showing that the number of flits passing through the router has a strong correlation to power consumption

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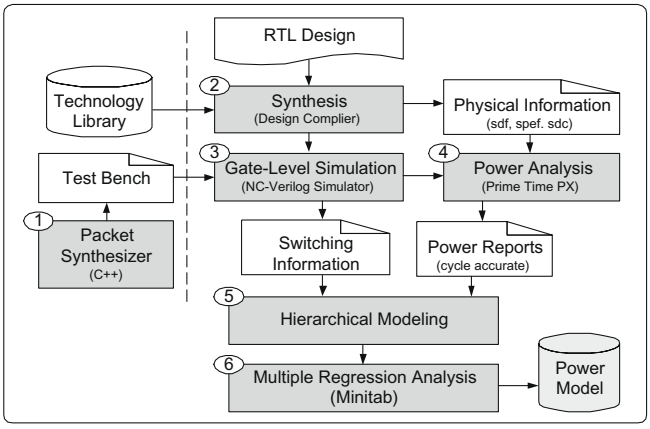


**Fig. 4.** Power model generation methodology.

as shown in Fig. 5. Based on this observation, four levels of hierarchical model are defined as shown in Fig. 6 by using the number of flits passing through the router as the unit of abstraction level. The model has mean value of power consumption for a router at Level 0 (L0) and has Idle and Active node at Level 1 (L1). The active node represents average power of a router when more than one flit is traversing the router. Similarly, the Idle node represents average power when the router is idle (i.e. no flit is passing through the router). Even though there are incoming flits to the router, the model just consider the number of outgoing flits in order to simplify the model. At Level 2 (L2), the Active node is decomposed into children nodes that reflect the number of outgoing flits. At the leaf level, the power macro model is derived including the effect of variables as described in the Section 4.1.

*4.2.2. Multiple regression analysis*

Average power for each node in the hierarchical power model would not be enough because it does not reflect the impact of actual data. In order to increase the accuracy of the power model, we created power macro model which reflects the contributions of the variables for power consumption.

From the simulation results, two important conclusions are drawn: (1) different payload affects differently the power because dynamic power is proportional to the switching activity of gates ($P = \frac{1}{2}\alpha C V_{dd}^2 f$, with $f$ the clock frequency, $\alpha$ the switching activity, $C$ the switch capacitance, and $V_{dd}$ the supply voltage). (2) the state of each outgoing port, whether it serves head or body flit, has a close relation to the overall power. In particular, state transition of outgoing port has a noticeable effect on its power consumption. Based on these observations, the power macro model of the router can be given as:

$$\widehat{P} = \alpha_0 + \alpha_H \cdot \psi_H + \alpha_S \cdot \psi_S + \alpha_{\Delta S} \cdot \psi_{\Delta S} \tag{2}$$

where $\psi_H$ is Hamming distance of outgoing flits; $\psi_S$ is the number of outgoing ports passing body flits; and $\psi_{\Delta S}$ is the number of state transitions of outgoing ports.

In Step 6, the switching information is compared with cycle accurate power reports and macro model templates for each node in the hierarchical model are generated using a *Perl* script. These templates consists of variables ($\Psi$) and power values

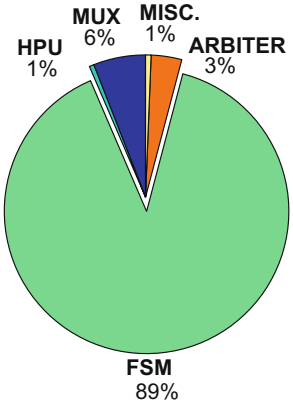


**Fig. 5.** Distribution of router power consumption.

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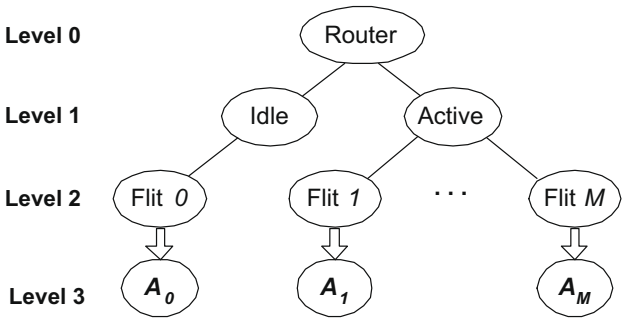


**Fig. 6.** Hierarchical power model for a router.

for every cycle of test bench and is applied to the MiniTab tool [27]. This tool performs multiple regression analysis to correlate the effect of each variables to power consumption finding coefficients for variables.

## 5. Accuracy of power model

In order to verify the accuracy of our power macro model for a router, the power macro model derived in the previous section was plugged into $4 \times 4$ mesh network. We applied four traffic patterns: uniform random; matrix transpose; bit complement; and bit reverse traffic patterns, which are generally used to evaluate the performance of a network, to the network and measured the average absolute cycle error (average of absolute error values at each cycle) in power estimated by the macro model compared to gate level analysis (see Table 1).

The L2 model ($\widehat{P}_{L2}$) which adopts the number of flit passing through the router as the abstraction unit showed less than 10.24% error under uniform random traffic. The L3 model which consider the effect of workload demonstrated more accuracy than L2 model. In order to observe the contribution of each variable on power consumption, four power models at L3 were evaluated: (1) $\widehat{P}_H$, which uses Hamming distance ($\psi_H$) as a variable; (2) $\widehat{P}_{S\Delta S}$ which, adopts state ($\psi_S$) and number of state transitions ($\psi_{\Delta S}$) as the variables; (3) $\widehat{P}_{HS\Delta S}$, which considers all of three variables; and (4) $\widehat{P}$, which adds empirical function to $\widehat{P}_{HS\Delta S}$. Adopting Hamming distance ($\psi_H$) as a variable reduces small error as compared to the L2 model. Introducing the state information including the state ($\psi_S$) and number of state transitions ($\psi_{\Delta S}$) reduced 51% of error compared to the L2 model, showing the strong correlation of the variables to the overall power consumption. Our power macro model ($\widehat{P}$), which considers all of three variables and adds empirical function to ($\widehat{P}_{HS\Delta S}$) demonstrated minimum error. It affirms that power model, which considers Hamming distance and state information, provides more accurate estimation.

In system level power exploration, average power also provides valuable information to system developer. Table 2 summarizes the average error of the power macro model with the same traffic patterns. Our power macro model demonstrated less than 1.5% average error as compared with gate level simulation.

Fig. 7 shows a snapshot of the power waveform generated by the power macro model (solid line) and gate level simulation (dotted line) using *PrimeTime* for a router located at (2,2) in a $4 \times 4$ mesh network. The L3 power waveform is very close

**Table 1**
Average absolute cycle error of power macro model estimation on $4 \times 4$ mesh network.

| Traffic | Level 2 (%) | Level 3 (%) | | | |
|---|---|---|---|---|---|
| Patterns | $e(\widehat{P}_{L2})$ | $e(\widehat{P}_H)$ | $e(\widehat{P}_{S\Delta S})$ | $e(\widehat{P}_{HS\Delta S})$ | $e(\widehat{P})$ |
| Uniform random | 10.24 | 10.18 | 5.07 | 5.04 | 4.76 |
| Matrix transpose | 8.67 | 8.66 | 4.37 | 4.31 | 3.90 |
| Bit complement | 8.35 | 8.36 | 3.47 | 3.50 | 2.77 |
| Bit reverse | 9.20 | 9.19 | 4.94 | 4.97 | 4.89 |

**Table 2**
Average error of power macro model estimation on $4 \times 4$ mesh network.

| Traffic | Level 2 (%) | Level 3 (%) | | | |
|---|---|---|---|---|---|
| Patterns | $e(\widehat{P}_{L2})$ | $e(\widehat{P}_H)$ | $e(\widehat{P}_{S\Delta S})$ | $e(\widehat{P}_{HS\Delta S})$ | $e(\widehat{P})$ |
| Uniform random | 1.74 | 1.69 | 0.20 | 0.42 | −1.43 |
| Matrix transpose | 4.97 | 5.03 | 1.13 | 1.27 | −0.19 |
| Bit complement | 3.69 | 3.85 | 1.28 | 1.43 | −0.24 |
| Bit reverse | 4.61 | 4.66 | 0.92 | 1.01 | −0.53 |

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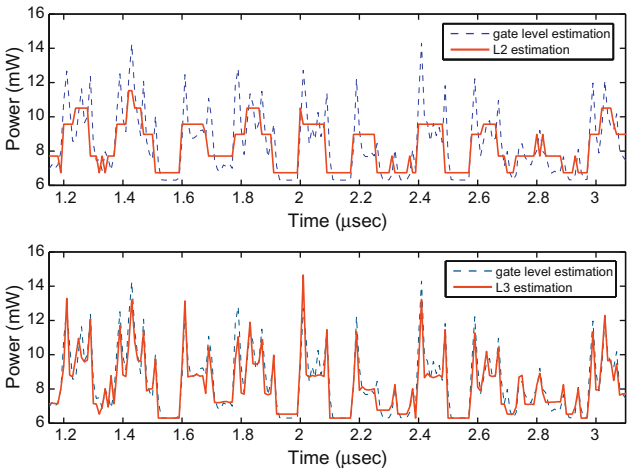


**Fig. 7.** Estimated and measured power waveforms at level 2 and level 3.

to the gate level power waveform, while the L2 power waveform shows less detailed estimation. The power model of the L3 allows extremely accurate power estimation with more than 1000× speed up over *PrimeTime* based estimation. As can be seen, the power estimates from the power model are highly correlated to the actual power consumption. Even though sporadic peaks are present, they do not affect the global behavior of the power model. The experimental results have confirmed the reliability of our power model, being the average absolute cycle error with respect to *PrimeTime* analysis within 5%.

## 6. System level power exploration

In this section, system level power estimation is performed using our power macro model to evaluate the relation between power consumption and different core mapping, which is not feasible at the gate level simulation due to the long simulation time and large generated file sizes. We use benchmarks from the SPLASH-2 [3] suite for a $7 \times 7$ network which provides the traffic among cores for each application without mapping detail. We implemented four different core mapping strategies named linear, zigzag, island, and random for $7 \times 7$ mesh network. The arrows in Fig. 8 reflect the increasing order of cores in the benchmark. Liner mapping allocates the cores from the left-uppermost one to the right-lowest one and zigzag mapping increases the order of core in zigzags. Island mapping imitates block allocation such that entire cores are divided into sub-blocks and each sub-block follows linear mapping. Finally, random mapping allocates each core in random. Even though these mapping strategies cannot realistically reflect the type of real application mapping, the experimental results for these mapping strategies demonstrates the utility of our model for system level power exploration. System designer can simulate various strategies to observe their influence on power quickly, which is not practically feasible with gate level simulation.

Fig. 9 shows the comparison of average power consumption for each benchmark. The power consumption of *fft* shows large difference between *island* and *linear* mappings (0.087 mw). Fig. 10 illustrates the average power consumption of each router in $7 \times 7$ mesh network for *fft* benchmark. While the *island* mapping has hot spot nodes (i.e. 7.34 mw at (6,4)) and shows large fluctuation of power dissipation in network, the *linear* mapping distributes the traffic load across the network reducing power consumption. The average power consumption of each test bench differs according to the mapping strategy. For instance, *fft* and *raytrace* have minimum power consumption with *linear* mapping while *water-nsquared* does with *island*

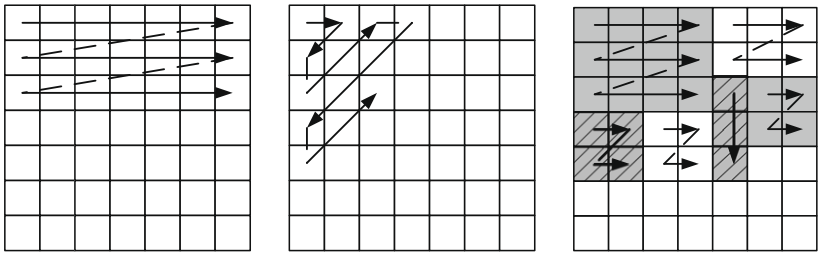


**Fig. 8.** Example of application mapping on $7 \times 7$ NePA.

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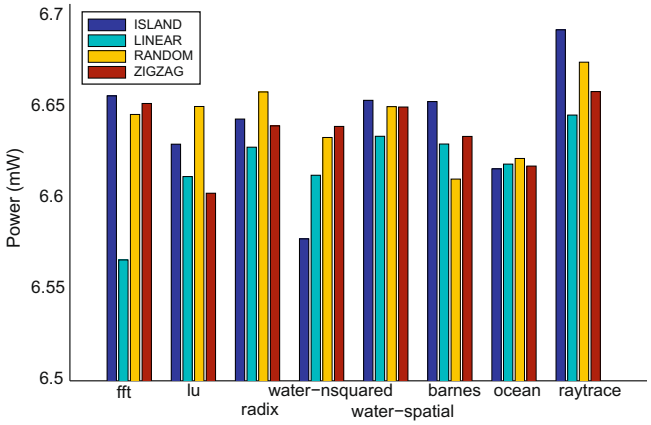


**Fig. 9.** Average power consumption for SPLASH-2 benchmark with different mapping strategies.

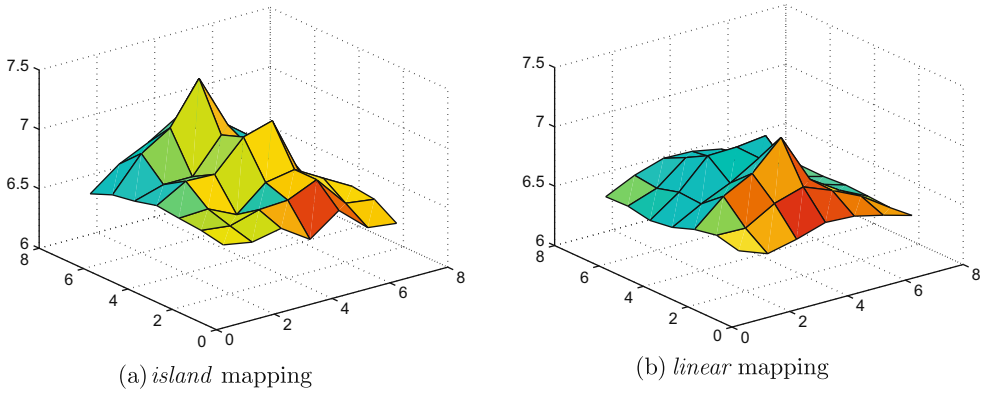


**Fig. 10.** Average power consumption of each router with *fft* benchmark in $7 \times 7$.

mapping. It affirms that optimization of core mapping can lead to significant power saving. Even though the differences in average power consumption is small, the power simulation with our model provides reasonable information to designers because the average error of our model is less than 0.028 mw as compared to the gate level estimation.

## 7. Conclusions

We presented a semi-automated power estimation framework that is capable of providing cycle accurate power profile to enable power exploration at system level for a Network-on-Chip router. A high level power macro model for a router was created using multiple regression analysis, and shown to have an average absolute cycle error of less than 5% compared to that of gate level estimation. In order to demonstrate the utility of our power model, we applied different core mapping strategies to $7 \times 7$ mesh network using SPLASH-2 benchmark and observed their influence on power consumption, which is not practically feasible with gate level simulation. We are in the process of preparing our power simulator for on-chip interconnection network for release, so it can be incorporated into power optimization such as power-aware compiler, core mapping, and scheduling, as well as other potential uses.

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