Chapter 3

Biasing of High-Gain Amplifiers

3.1 Biasing of Common-Emitter/Common-Source Amplifiers

So far in our small-signal analyses we have assumed that there has been a well-defined dc operating point – that is, the dc voltages and currents are known and correspond to the desired region of operation for the transistor (usually forward-active for a BJT and saturation for a MOSFET). Once this operating point is known, the small-signal transistor parameters (e.g., \( g_m, r_o \)) can easily be calculated to find the desired small-signal performance parameters (e.g., voltage gain, input/output resistance). Of course, it is up to the designer to make sure that the operating point is well-defined even when the temperature and processing parameters vary. This is seldom trivial.

Let us consider once again a common-emitter amplifier, shown in Fig. 3.1(a). In this simple biasing arrangement discussed earlier, we set the desired dc collector current \( I_C \) by applying a voltage source \( V_{BE} \) across the base-emitter junction of the transistor. We know that \( I_C \) is an exponential function of \( V_{BE} \), illustrated by curve X in Fig. 3.2(a). Suppose that we have chosen for our design \( V_{CC} = 3.3 \text{ V}, R_C = 4 \text{ k} \Omega \), and dc collector current \( I_C = 400 \mu \text{A} \). With these values the dc value of \( V_{out} \) is calculated to be 1.7 V. Notice that at this operating point the transistor is well within its forward active region and that \( V_{out} \) can swing nearly symmetrically.

From the \( I_C \) vs. \( V_{BE} \) transistor characteristic shown in Fig. 3.2(a), where \( V_T = 26 \text{ mV} \) and \( \alpha P_{Es} = 5.8 \times 10^{-15} \) A, \( I_C = 400 \mu \text{A} \) corresponds
Figure 3.1: (a) Voltage source biasing of common-emitter amplifier; (b) emitter degeneration added; (c) bypass capacitor $C_E$ added.

to $V_{BE} \approx 649$ mV. Now suppose that this $i$-$v$ characteristic were shifted slightly to the left by 16 mV, resulting in curve $Y$ of Fig. 3.2(a). Such a shift could be caused, for example, by the chip temperature increasing by about 8°C. In general, such shifts (either to the right or left) must always be anticipated since device characteristics cannot be predicted with arbitrary precision and because integrated circuits must operate properly over a wide range of temperatures\(^1\). Alternatively, even if the device itself were exactly represented by curve $X$, it’s quite possible that the voltage source value itself could vary by a few millivolts. In either case, such a shift in the characteristic is common and must always be anticipated in the amplifier design. In this example, notice that the small shift of 16 mV in the transistor characteristic results in a very large change in biasing: $I_C$ increases from 400 $\mu$A to 640 $\mu$A – more than a 50% increase! This would significantly affect the small-signal behavior of this amplifier; or worse, it might also cause the transistor to be in the wrong region of operation. For this example, a shift of 16 mV at the input would cause the dc value of $V_{out}$ to decrease from 1.7 V to 0.74 V, thus biasing the transistor much closer to the saturation region and resulting in severely limited output swing.

So that the dc operating point is less sensitive to small perturbations,

\(^1\)For example, ICs used in commercial applications must operate between 0°C and 70°C C.
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![Graph](attachment:image.png)

**Figure 3.2:** (a) Exponential $i$-$v$ characteristic; (b) biasing with emitter degeneration.
we would prefer a more robust way of biasing the Fig. 3.1(a) amplifier. To alleviate this problem, let us consider placing a resistor in series with the emitter, as shown in Fig. 3.1(b). Note that the dc voltage source connected to the base is labeled $V_B$ rather than $V_{BE}$ since it is no longer connected directly across the transistor’s base-emitter junction. In order to determine this circuit’s dc operating point, we first write the following KVL equation corresponding to the loop consisting of $V_B$, the base-emitter junction, and $R_E$:

$$V_B = V_{BE} + I_E R_E$$

(3.1)

We now wish to find appropriate values of $V_B$ and $R_E$ so that $I_C$ is again set to 400 $\mu$A. Assuming that $I_E = I_C$ (i.e., $\alpha_F = 1$) and setting $V_{BE} = 649$ mV and $I_E = 400$ $\mu$A into the above equation, we have:

$$V_B = 0.649 \text{ V} + (400 \text{ } \mu\text{A}) \cdot R_E$$

(3.2)

Since we have one equation but two unknowns, we are free to choose either $V_B$ or $R_E$ arbitrarily. For reasons that will be clear shortly, we should choose $R_E$ large enough so that $R_E >> 1/g_m$. For $I_C = 400$ $\mu$A, we have:

$$\frac{1}{g_m} = \frac{26 \text{ mV}}{400 \text{ } \mu\text{A}} = 65 \Omega$$

(3.3)

Let us then choose $R_E = 1.5$ k$\Omega$. Substituting this value back into (3.2), we obtain $V_B = 1.249$ V. Based on these parameters, we can rewrite (3.1) as:

$$1.249 \text{ V} = V_{BE} + (1500 \Omega) \cdot I_E$$

(3.4)

This load-line characteristic, which has slope $1/R_E$, is plotted in Fig. 3.2(b). The intersection of this line with the exponential transistor characteristic curve $X$ yields the same operating point as the one illustrated in Fig. 3.2(a), corresponding to the Fig. 3.1(a). However, if we apply the same perturbation as before (curve Y), we see that now the operating point is nearly unchanged. The reason for this is in the region where the base-emitter junction is forward biased, the slope of the transistor $i-v$ characteristic (this is by definition $g_m$) is much larger than that of the load line, which was arranged by setting $R_E >> 1/g_m$, as mentioned earlier.

We now have very robust biasing. However, there is a price to be paid for this improvement: The presence of resistor $R_E$ will also affect the small-signal gain. To understand this behavior, we first do a cursory qualitative analysis on the Fig. 3.1(b) circuit. As discussed in the analysis of the common-collector amplifier in Chapter 2, the emitter current $I_E$ is given by:

$$I_E \approx \frac{V_B - V_{BE(on)}}{R_E}$$

(3.5)
\[ V_{\text{OUT}} = V_{\text{CC}} - I_C R_C \]
\[ \approx V_{\text{CC}} - (V_B - V_{\text{BE(on)}}) \cdot \frac{R_C}{R_E} \quad (3.6) \]

Thus from this simplified analysis, we estimate the small-signal voltage gain to be approximately \( -R_C/R_E \).

To obtain a more precise expression – one that would take into account the effects of all of the various small-signal parameters – let us consider the small-signal circuit shown in Fig. 3.3, which corresponds to the Fig. 3.1(b) circuit. Note that, due to the presence of \( R_E \), there are no resistors connected in parallel in this circuit configuration. The KCL equations at the output (collector) and emitter nodes, respectively, are given by:

\[ \frac{v_{\text{out}}}{R_C} + \frac{1}{r_o} (v_{\text{out}} - v_e) + g_m v_\pi = 0 \quad (3.7) \]
\[ \frac{v_e}{R_E} + \frac{1}{r_o} (v_e - v_{\text{out}}) - g_m v_\pi + \frac{1}{r_\pi} (v_e - v_{\text{in}}) = 0 \quad (3.8) \]

Gathering common terms in (3.7) and (3.8) and making the usual substitution \( v_\pi = v_{\text{in}} - v_e \), we have:

\[ v_{\text{out}} \left( \frac{1}{R_C} + \frac{1}{r_o} \right) - v_e \left( g_m + \frac{1}{r_o} \right) + g_m v_{\text{in}} = 0 \quad (3.9) \]
\[ v_e \left( \frac{1}{R_E} + \frac{1}{r_o} + \frac{1}{r_\pi} \right) - \frac{v_{out}}{r_o} - v_{in} \left( \frac{g_m + \frac{1}{r_\pi}}{r_o} \right) = 0 \]  \hspace{1cm} (3.10)

We will now make some simplifications to the above equations based on inequalities discussed in Chapter 2. Let us assume the following:

\[ r_o >> \frac{1}{g_m} \]
\[ r_o >> R_C \text{ and } R_E \]
\[ r_\pi >> \frac{1}{g_m} \]

Applying the above inequalities to (3.9) and (3.10), we can approximate the equations by:

\[ \frac{v_{out}}{R_C} - g_m v_e + g_m v_{in} = 0 \]  \hspace{1cm} (3.11)
\[ v_e \left( \frac{1}{R_E} + g_m \right) - \frac{v_{out}}{r_o} - g_m v_{in} = 0 \]  \hspace{1cm} (3.12)

Combining the above two equations we have:

\[ v_{out} \left( \frac{1}{g_m R_C R_E} + \frac{1}{R_C} - \frac{1}{r_o} \right) + \frac{v_{in}}{R_E} = 0 \]  \hspace{1cm} (3.13)

Once again noting out assumption that \( r_o >> R_C \), the above equation can be further simplified to:

\[ \frac{v_{out}}{v_{in}} = -\frac{R_C/R_E}{1 + \frac{1}{g_m R_E}} \]  \hspace{1cm} (3.14)

From the above expression we see that the expected gain of \(-R_C/R_E\) from our previous qualitative analysis is verified, but only under the condition that \( g_m R_E >> 1 \). To gain additional insight into this expression, we multiply the numerator and denominator of (3.14) by \( g_m R_E \), rewriting the voltage gain as:

\[ A_v = -\frac{g_m R_C}{1 + g_m R_E} \]  \hspace{1cm} (3.15)

Note that the numerator of (3.15) is the gain of the original common-emitter amplifier before \( R_E \) has been placed in series with the emitter; the expression \((1 + g_m R_E)\) in the denominator of (3.15) gives the reduction in gain due to the insertion of \( R_E \). For this reason such an insertion is known as “emitter degeneration.” Resistor \( R_E \) functions to make the dc operating point more robust while reducing the magnitude of the voltage gain.
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To gain some insight into how this expression affects the circuit behavior, let us once again consider the graphs in Fig. 3.2(b). As seen in these graphs, the robustness of the operating point is dependent on the slope of the transistor’s $I_C$ vs. $V_{BE}$ curve, $g_m$, being much larger than the magnitude of the slope of the linear curve (corresponding to the resistor), $1/R_E$. Thus we require:

$$g_m \gg \frac{1}{R_E}$$

$$\implies g_m R_E \gg 1$$

(3.16)

If we write this expression in terms of dc biasing parameters, we have:

$$g_m R_E = \frac{I_C}{V_T} \cdot R_E = \alpha_F \cdot \frac{I_F R_E}{V_T}$$

(3.17)

In other words, (3.16) is satisfied when the voltage drop across $R_E$ is much larger than $V_T$.

Note that the above derivations also hold, with some minor modifications, for the common-source amplifier as well. The details have been left as an exercise. The effects of considering $r_{\pi}$ and $r_o$ on the gain expression have also been left as an exercise.

Let us summarize what has been discussed so far.

- A common-emitter or common-source amplifier is capable of moderate voltage gain – approximately 60 for the common-emitter and 8 for the common-source, based on the examples from the previous chapter.

- Setting the dc biasing by forcing a voltage directly across the base-emitter or gate-source terminals renders the operating point far too sensitive to PVT variations to be practically useful.

- Using emitter- (or source-) degeneration renders the operating point more robust, but at the expense of reducing the voltage gain.

It would be desirable to find a circuit structure that would exhibit both the robustness of the dc biasing and the high small-signal gain. If the signal to be amplified were known to be made up of a limited range of frequencies, we might be able to take advantage of frequency-selective circuit components. Let us now consider the circuit shown in Fig. 3.1(c), where the emitter-degenerated amplifier shown in Fig. 3.1(b) has been augmented with an additional capacitor $C_E$ inserted in parallel with degeneration resistor $R_E$. Since a capacitor behaves like an open circuit at dc, clearly this
circuit's dc biasing is identical to that of Fig. 3.1(b) – thus it is robust as discussed earlier. However, at sufficiently high frequencies, a capacitor behaves like a short circuit – that is, at these frequencies the degeneration resistor is effectively shorted out and the emitter terminal behaves like a small-signal ground. Thus at high frequencies the small-signal gain will be identical to that of the original common-emitter stage in Fig. 3.1(a).

We have used a capacitor in the circuit to separate the small-signal and dc biasing behavior of the circuit. There are two tradeoffs here:

1. There is a lower bound on the frequency that can be applied to the circuit for which there is high gain, as illustrated in the gain vs. frequency plot shown in Fig. 3.4. (The values of critical frequencies $\omega_L$ and $\omega_H$ are left as a homework assignment.)

2. The lower the expected input frequency, the larger $C_E$ must be. For example, if we were to apply an audio signal to the amplifier, where the frequency range is between 20 Hz and 20 kHz and the transconductance $g_m$ were on the order of 1 mS, $C_E$ would have to be in the $\mu$F range. This is far too large to be integrated in a chip. Thus, this capacitor would have to be connected externally, and an extra pin would be needed in order to connect this external capacitor to the emitter terminal on the chip. This would require additional space on the circuit board and incur additional fabrication costs, both of which are undesirable.

We now can consider the following question: *Is it possible to separate the dc biasing and small-signal behaviors without requiring a large capacitor in the circuit? This will be considered in the next section.*

### 3.2 Differential Pair Structure

We now consider a pair of identical common-emitter stages with emitter degeneration as shown in Fig. 3.5(a). If we apply the same dc voltage $V_B$ to both transistor bases, clearly the biasing is identical for both sides of the pair. Thus all dc voltages and currents (e.g., $I_C$ and $V_E$) are identical on both sides. Let us apply two small-signal voltage sources to the two amplifiers, with equal amplitudes but with opposite signs – that is, the voltage applied on the left is $+v_{in}/2$ and the voltage on the right is $-v_{in}/2$, as shown in Fig. 3.5(b). Since the biasing is identical for both amplifiers, then for each small-signal current or voltage on the left-hand amplifier, there will be an equal and opposite corresponding small-signal quantities on the right-hand
ampfiﬁer, as illustrated in Fig. 3.5(b). Let us focus our attention on the small-signal emitter voltages, \( \pm v_e \). As discussed previously, the emitter degeneration resistors result in more robust biasing, but signiﬁcantly lower gain; the lower gain is directly related to the presence of small-signal voltages \( \pm v_e \).

How might we eliminate these small-signal voltages, thereby perhaps increasing the small-signal gain? One way might be to simply short-circuit the emitters of the two amplifiers, as shown in Fig. 3.5(c). (Note that by symmetry, this short-circuit connection will not change the original dc operating point.) By doing this, we now constrain the two emitter voltages as follows:

\[
+ v_e = - v_e \tag{3.18}
\]

Obviously the only solution to (3.18) is \( v_e = 0 \). In other words, the combination of anti-symmetry from the applied small-signal voltages and the short circuit between the two emitters results in the emitters behaving like a small-signal ground! Thus, without performing any further calculations, we can then conclude that the small-signal behavior of the Fig. 3.5(b) circuit is identical to the standard common-emitter amplifier:

\[
\begin{align*}
  v_c &= - g_m (R_C | r_o) \cdot \left( \frac{1}{2} v_{in} \right) \\
  -v_c &= - g_m (R_C | r_o) \cdot \left( - \frac{1}{2} v_{in} \right) \tag{3.19}
\end{align*}
\]
Figure 3.5: Differential pair evolution.
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Note that this gain expression holds for either side of the Fig. 3.5(c) circuit, which we have redrawn as the circuit in Fig. 3.5(d). This structure is commonly known as a “differential pair” and since the gain is taken between the differential output and differential input, the circuit is said to function as a “differential amplifier.” By assigning $v_{out}$ to be the small-signal voltage difference across the collectors as illustrated in Fig. 3.5(d), and taking the difference between the two equations in (3.19), then we have:

$$v_{out} = -g_m(R_C | v_o) \cdot v_{in}$$  \hspace{1cm} (3.20)

To summarize, the differential pair allows for both robust biasing and large gain without requiring any additional capacitors. This remarkable property is possible due to the application of a differential input small-signal voltage to a pair of input terminals, which causes the emitter degeneration resistor to be transparent to the signal.

3.3 Differential-Mode and Common-Mode Signals

In the previous section we have motivated the use of pairs of nodes to define inputs and outputs. In general, we could apply any two arbitrary signals $v_{in+}$ and $v_{in-}$ to the input terminals as shown in Fig. 3.6(a). We now define, for any such pair of signals, its differential-mode component $v_{in(dm)}$ and its common-mode component $v_{in(cm)}$:

$$v_{in(dm)} \equiv v_{in+} - v_{in-}$$  \hspace{1cm} (3.21)

$$v_{in(cm)} \equiv \frac{1}{2} (v_{in+} + v_{in-})$$

In other words, the differential-mode component of a pair of signals is the difference between them; the common-mode component of a pair of signals is their average. We can invert the above relations to give:

$$v_{in+} = v_{in(cm)} + \frac{1}{2} v_{in(dm)}$$  \hspace{1cm} (3.22)

$$v_{in-} = v_{in(cm)} - \frac{1}{2} v_{in(dm)}$$

Similar definitions hold for $v_{out(cm)}$ and $v_{out(dm)}$ as well. Thus any arbitrary pair of signals can always be decomposed into a differential-mode component and a common-mode component. Why would we want to do this? It turns
out that directly solving the Fig. 3.6(a) circuit for an arbitrary pair of inputs is tedious – the small-signal model (not shown) for this circuit would contain two transistors and an additional internal node \( v_e \), which would be difficult and time-consuming to solve. But if we instead solve two simpler circuits – one to which only a differential-mode component is applied and another to which only a common-mode component is applied – our task is much easier and we get some additional insights into the circuit’s operation. Since these are linear small-signal analyses, the overall response will be just the sum of the effects of the two individual behaviors.

**Differential-mode Behavior**

We have already qualitatively analyzed the Fig. 3.6(a) differential pair circuit for differential-mode inputs. We will now do a more rigorous analysis. Consider the differential amplifier with differential inputs applied as shown in Fig. 3.6(b). As mentioned earlier, by symmetry any small-signal voltage or current on one side of the amplifier appears on the other side with exactly the same magnitude but opposite sign. In particular, if the small-signal voltage on the emitter of the left-hand transistor were \( v_e \), then the voltage on the emitter of the right-hand transistor would be \(-v_e\), as illustrated in the figure. However, the two emitters are connected together, which implies that the two small-signal voltages must be the same. Thus, as we concluded before, the only possible solution is \( v_e = 0 \). The corresponding small-signal diagram, shown in Fig. 3.6(c), needs to only include one half of the circuit, since by symmetry the other half displays exactly the same voltages and currents except for a sign change, and has the transistor emitter connected to a small-signal ground. Notice that this small-signal circuit is identical to the simple one-transistor common-emitter amplifier analyzed in the previous chapter, with the differential-mode gain the same as given in (3.20). we will call this the differential-mode gain \( A_{dm} \), defined as:

\[
A_{dm} \equiv \frac{v_{out(dm)}}{v_{in(dm)}} \bigg|_{v_{n(em)}=0} \tag{3.23}
\]

Thus we can write:

\[
A_{dm} = -g_m (R_C || r_o) \approx -g_m R_C \tag{3.24}
\]

Substituting dc biasing parameters and physical constants into the small-signal parameters in (3.24), we have:

\[
A_{dm} \approx -\frac{I_C R_C}{V_T} = -\frac{V_{CC} - V_{OUT}}{V_T} \tag{3.25}
\]
Figure 3.6: Differential-mode and common-mode analysis of a differential pair.
Thus the differential-mode gain is limited by the value of the power supply and the dc output voltage.

Common-mode Behavior

We'll now consider the differential amplifier with only common-mode signals applied to the inputs, as illustrated in Fig. 3.6(d). We can once again make a simplification to this circuit by exploiting symmetry, this time by first splitting resistor $R_{EE}$ into two parallel resistors, each with double the value as illustrated in the figure. For common-mode signals, any small-signal voltage or current on one side must be exactly the same (with the same sign) on the other side. In particular, if we consider a current $i_x$ flowing as shown in the left half of the circuit, then an identical current must also be flowing in the right half of the circuit. However, KCL constrains the sum of these two currents $2i_x$ to be zero; thus, the only possible solution is $i_x = 0$.

In other words, in the presence of common-mode signals, the short circuit connected between the two emitters carries no small-signal current and its removal will have no effect on the circuit’s behavior. After removing this branch, once again we have two separate, identical half-circuits remaining and it suffices just to analyze the circuit common-mode half-circuit shown in Fig. 3.6(e). As discussed earlier, the gain of this circuit is the same as that given in (3.15):

$$A_{cm} = -\frac{g_m R_C}{1 + g_m R_{EE}}$$  \hspace{1cm} (3.26)

In this expression, for $g_m R_{EE} \gg 1$, we have:

$$A_{cm} \approx -\frac{R_C}{2R_{EE}}$$  \hspace{1cm} (3.27)

Substituting dc biasing parameters and physical constants into the small-signal parameters in (3.26), we have:

$$A_{cm} = -\frac{I_c R_C}{1 + 2I_c R_{EE}} = -\frac{V_{CC} - V_{OUT}}{V_T + (V_B - V_{BE(on)})}$$  \hspace{1cm} (3.28)

Common-mode Rejection

We have now clearly determined that the gain of the differential amplifier is higher for differential-mode signals than for common-mode signals. This quality is actually very desirable – we can arrange to have the signal intended for amplification to be applied in a differential fashion. Other undesirable
3.3. \textit{DIFFERENTIAL-MODE AND COMMON-MODE SIGNALS}

Signals that we would prefer not to have amplified - e.g., disturbances from other circuitry, noise from the power supply - normally are coupled to the amplifier inputs as common-mode signals. Thus it is desirable to have a large \textit{common-mode rejection ratio} (CMRR), defined as:

\[
\text{CMRR} \equiv \frac{|A_{dm}|}{A_{cm}}
\]  
(3.29)

Plugging expressions in (3.24) and (3.26) into (3.29), we have:

\[
\text{CMRR} = 1 + 2g_m R_{EE} = 1 + \frac{2I_C R_{EE}}{V_T}
\]  
(3.30)

Note that the numerator $2I_C R_{EE}$ in the above equation is exactly the same as the dc voltage across resistor $R_{EE}$, which can also be written as $V_B - V_{BE}$. Thus, (3.30) can be rewritten as:

\[
\text{CMRR} = 1 + \frac{V_B - V_{BE}}{V_T}
\]  
(3.31)
Example 4.1: We wish to design a BJT differential amplifier with $V_{CC} = 3.3$ V, input dc biasing of 1 V, the collector current in each transistor is 500 $\mu$A, and the output exhibiting the maximum possible output swing. Then find $A_{dm}$, $A_{cm}$, and CMRR. Assume $V_{BE(on)} = 0.7$ V, $V_{BC(on)} = 0.5$ V, and $\beta = 100$.

Referring to the Fig. 3.6(a) circuit, in order to realize the desired collector currents, we first note that since the dc voltage $V_B = 1$ V, the emitter voltage $V_E = 0.3$ V. Having the collector current of 500 $\mu$A requires that the sum of the emitter currents, which is conducted in $R_{EE}$, is:

$$2I_E = \frac{(2)(500 \text{ } \mu\text{A})}{0.99} = \frac{0.3 \text{ V}}{R_{EE}}$$

$$\Rightarrow R_{EE} = 297 \text{ } \Omega$$

Since the minimum voltage at either output will be 0.5 V and it is specified to have the highest possible, swing, then the optimum dc output voltage will be:

$$V_{out(opt)} = \frac{1}{2} [0.5 \text{ V} + 3.3 \text{ V}] = 1.9 \text{ V}$$

Thus we can write:

$$I_C R_C = V_{CC} - V_{out(opt)} = 1.4 \text{ V}$$

$$\Rightarrow R_C = \frac{V_{CC} - V_{out(opt)}}{I_C} = \frac{3.3 \text{ V} - 1.9 \text{ V}}{500 \text{ } \mu\text{A}} = 2.8 \text{ k}\Omega$$

To find the gains and CMRR, we can write the following:

$$A_{dm} = -g_m R_C = -\frac{I_C R_C}{V_T} = -\frac{1.4 \text{ V}}{0.026 \text{ V}}$$

$$A_{cm} = -\frac{I_C R_C}{1 + \frac{2I_C R_{EE}}{V_T}} = -\frac{1.4 \text{ V}}{1 + \frac{2(0.48 \text{ V})}{0.026 \text{ V}}} = -4.33$$

$$\text{CMRR} = \frac{A_{dm}}{A_{cm}} = 12.4$$
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To gain some insight into the importance of these various gain parameters, consider the differential amplifier shown in Fig. 3.7(a) that is driven with a pair of differential signals that are connected through long cables. Suppose that a disrupting signal $v_{\text{noise}}$ is capacitively coupled into the inputs through the cable as illustrated in the figure. Since this signal is coupled in to both inputs symmetrically, it affects the common-mode component of the input signal.

For $v_{\text{in}}$ set to a 1 kHz sine wave with 10 mV amplitude and $v_{\text{noise}}$ set to a 2 kHz sine wave with a 5 mV amplitude, the signals appearing at $V_{\text{in}+}$, $V_{\text{in}-}$, and their differential-mode and common-mode components are shown in Fig. 3.7(b). Note that although the single-ended waveforms are distorted – that is, they exhibit significant components other than the 1 kHz sine wave – their differential-mode component is sinusoidal.

The signals appearing at $V_{\text{out}+}$, $V_{\text{out}-}$, and their differential-mode and common-mode components are shown in Fig. 3.7(c). In comparing the input and output waveforms – particularly the ratio of the differential-mode and common-mode components in each – the effect of the large common-mode rejection ratio is evident.
Figure 3.7: (a) Differential amplifier; (b) input signals; (c) output signals.
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Example 4.2: We wish to design a MOSFET differential amplifier with $V_{DD} = 1.8$ V, input dc biasing of 0.9 V, each transistor having $I_D = 150$ µA and $V_{GS} - V_t = 0.1$ V, and the output exhibits the maximum possible output swing. Then find $A_{dm}$, $A_{cm}$, and CMRR. Assume $V_t = 0.5$ V and $k' = 150$ µA/V².

In order to realize the desired drain currents, we first note that since the dc voltage $V_G = 0.9$ V, the source voltage $V_S = 0.3$ V. Having the drain current of 150 µA requires that the sum of the source currents, which is conducted in $R_{SS}$, is:

$$2I_D = 300 \text{ µA} = \frac{0.3 \text{ V}}{R_{SS}}$$

$$\rightarrow R_{SS} = 1 \text{ kΩ}$$

Since the minimum voltage at either output will be $V_G - V_t = 0.4$ V, the optimum dc output voltage will be:

$$V_{out(opt)} = \frac{1}{2} [0.4 \text{ V} + 1.8 \text{ V}] = 1.1 \text{ V}$$

Thus we can write:

$$I_D R_D = V_{DD} - V_{out(opt)} = 0.7 \text{ V}$$

$$\rightarrow R_D = \frac{V_{DD} - V_{out(opt)}}{I_D}$$

$$= \frac{1.8 \text{ V} - 1.1 \text{ V}}{150 \text{ µA}} = 4.67 \text{ kΩ}$$

To find the gains and CMRR, we can write the following:

$$A_{dm} = -g_m R_D = -\frac{2I_D R_D}{V_{GS} - V_t} = -\frac{(2)(0.7 \text{ V})}{0.1 \text{ V}}$$

$$= -14$$

$$A_{cm} = -\frac{2I_D R_D}{1 + \frac{U_D R_{SS}}{V_{GS} - V_t}} = -\frac{(2)(0.7 \text{ V})}{1 + \frac{4.67 \text{ kΩ}}{0.1 \text{ V}}}$$

$$= -2$$

**CMRR** = $\left| \frac{A_{dm}}{A_{cm}} \right| = 7$
Limitations from Biasing

Equation (3.31) explicitly shows that the CMRR is limited by dc biasing constraints in the circuit – in particular, the quantity $V_B - V_{BE}$ is limited by the value of $V_{CC}$ and the desired signal swing. Let us explore this in more detail by analyzing the large-signal behavior of the differential pair in Fig. 3.6(a). In order for this circuit to operate properly, both transistors must be in the forward-active region. Thus the maximum dc voltage that can appear on either of the two outputs must be $V_{CC}$, since any voltage higher than $V_{CC}$ would cause the collector current to be negative, which would imply that the transistor is not operating in the forward active region. The minimum dc voltage that can appear on either output occurs when the transistor goes into the saturation region; i.e., when $V_{BC}$ becomes $V_{BC(on)}$. In summary, we can give the following range for the dc value of either output voltage:

$$V_B - V_{BC(on)} < V_{OUT} < V_{CC}$$  (3.32)

When designing an amplifier it is often desirable to have the maximum possible voltage range for which the gain stays high, which is possible only when the transistors remain in their appropriate region of operation. This is accomplished by setting the dc operating point so that the dc output voltages are exactly in the middle of the range given in (3.32). As an example, for the Fig. 3.6(a) circuit let $V_{CC} = 3.3V$, $V_B = 1.3V$, $V_{BE(on)} = 0.7V$ and $V_{BC(on)} = 0.5V$. Then the optimum dc voltage at the output would be given by:

$$V_{OUT(opt)} = \frac{1}{2} \left[V_{CC} + V_B - V_{BC(on)}\right] = 2.05V$$  (3.33)

All of these node voltages are labeled in the differential pair schematic shown in Fig. 3.8. Our only task now is to find the values of resistors $R_C$ and $R_{EE}$ in the circuit. For our example we will choose $R_{EE} = 1k$ which sets $I_{EE} = 600\mu A$ and $I_C = 300\mu A$ (assuming large transistor $\beta$). Thus we must set $R_C = 4.17k$ in order to satisfy (3.33).

The voltage swing for this example would be as illustrated in Fig. 3.9(a). Notice that the swing is symmetric around the dc operating point, as desired, giving the overall voltage swing as 2.5 V peak-to-peak. Suppose that we increased the value of $R_C$ from 4.17 kΩ to 5.67 kΩ. The emitter and collector currents would remain the same, since they are set by $V_B$ and $R_{EE}$; thus the result of this change would be that the dc value of $V_{OUT}$ would decrease from 2.05 V to 1.60 V. The maximum voltage swing for this case is illustrated in Fig. 3.9(b). In this case the minimum voltage is reached before the maximum voltage; thus the swing is limited to only 1.6 V peak-to-peak.
3.3. DIFFERENTIAL-MODE AND COMMON-MODE SIGNALS

![Diagram of a differential pair with dc voltages labeled.](image)

Figure 3.8: Differential pair with dc voltages labeled.

![Diagram of output voltage swing for optimum biasing and non-optimum biasing.](image)

Figure 3.9: (a) Output voltage swing for optimum biasing; (b) non-optimum biasing.
Since the value of $V_{OUT}$ has been fixed as a result of large-signal constraints, then from (3.25) the small-signal gain is also fixed. For this example, we have:

$$A_{dm} = -g_m R_C = -\frac{V_{CC} - V_{OUT}}{V_T} = -\frac{3.3 \text{ V} - 2.05 \text{ V}}{0.026 \text{ V}} = -48 \quad (3.34)$$

Likewise, for the CMRR, we have:

$$CMRR = 1 + 2g_m R_{EE} = 1 + \frac{V_B - V_{BE}}{V_T} = 1 + \frac{1.3 \text{ V} - 0.7 \text{ V}}{0.026 \text{ V}} = 24 \quad (3.35)$$

The values of $A_{dm}$ and CMRR found from (3.34) and (3.35) are considered to be modest values. In fact, we’d prefer to have both of these parameters higher by at least an order of magnitude. In the next section we will explore ways to improve the differential amplifier circuit such that these values are higher.

### 3.4 Overcoming Limitations Set by Resistors

As discussed earlier, the limits on the gain and CMRR come from biasing constraints. The primary reason for this is that resistors $R_C$ and $R_{EE}$ must conduct both dc and small-signal current simultaneously; thus the limitations from the dc biasing directly impinge on the small-signal behavior. To resolve this trade-off, let us imagine that we could somehow separate the small-signal current from the dc current and have them conducted in separate paths. This idea, applied to resistor $R_{EE}$, is illustrated in Fig. 3.10, where $R_{EE}$ has been replaced by the parallel combination of dc current source $I_{EE}$ and resistor $r_{EE}$, assumed to be much larger than $R_{EE}$ in the original differential amplifier. The idea here is to have $I_{EE}$ conduct only the dc current and to have $r_{EE}$ conduct mostly the small-signal current (for this reason we use a lower-case $r$ in the name of the resistor). Since the dc voltage drop between the emitters and ground is no longer proportional to $r_{EE}$, the value of this resistor can be as large as we wish, thereby allowing a CMRR that is no longer limited by dc biasing constraints!

For this new circuit we can find the expression for CMRR:

$$CMRR = 1 + 2g_m r_{EE} = 1 + \frac{2I_{CPEE}}{V_T} \quad (3.36)$$

In the above expression, the factor $I_{CPEE}$ is not a dc voltage drop found in the Fig. 3.10 circuit; therefore there is no limitation on the CMRR due to
biasing constraints. A fair question now is: how do we realize a dc current source? This question, as well as how to increase $A_{dm}$, will be addressed in the next chapter.
CHAPTER 3. BIASING OF HIGH-GAIN AMPLIFIERS