Chapter 4

Design of Current Sources

4.1 Introduction

As discussed in the end of the previous chapter, the availability of a current source would be very desirable in order to improve both the CMRR and the differential-mode gain of a differential amplifier. In this chapter we will discuss some practical ways in which this can be done – in particular, we will see how a single transistor can behave as a good approximation to an ideal current source.

We begin by considering the behavior of an ideal current source, illustrated in Fig. 4.1(a). Such a one-port conducts a constant specified current $I_S$, regardless of port voltage $V$; thus its v-i characteristic is simply a horizontal line. Since this holds even when $V$ and $I$ are of opposite signs, note that this element is not passive – that is, the characteristic is not limited to the first and third quadrants. Thus we can expect that the characteristic as shown in Fig. 4.1(a) cannot be exactly realized by passive elements.

A somewhat less ideal (but more realistic) version of a current source is shown in Fig. 4.1(b), where a resistor $R_S$ has been placed in parallel with the ideal current source. As long as $R_S$ is large, we still obtain an approximation of current source behavior – that is, the line is nearly horizontal with small slope $1/R_S$ so that there is some small variation in port current $I$ as port voltage $V$ changes.

Let us now consider a current source realized by a BJT as shown in Fig. 4.1(c). Assume that the voltage source $V_{BE}$, connected across the transistor's base-emitter junction, has been set so that when the transistor is in the forward active region, it conducts collector current $I_C \approx I_S$. We see that the portion of the curve corresponding to $V > V_{CE(sat)}$ looks nearly
Figure 4.1: (a) Ideal current source; (b) Ideal current source with parallel resistance; (c) Realization of a current source using a BJT; (d) Realization of a current source using a MOSFET.
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identical to that in Fig. 4.1(b). Thus we can conclude that a single transistor behaves like the current source/resistor parallel combination with the transistor $r_o$ playing the role of $R_S$ under the condition that port voltage $V > V_{CE(sat)}$. Similar behavior is exhibited by the n-channel MOSFET implementation shown in Fig. 4.1(d). The constraint on the port voltage $V$ for this implementation is $V > V_{GS} - V_t$.

We can conclude that a single transistor with a set base-to-emitter (or gate-to-source) voltage can behave similar to a current source in parallel with a large resistor, over a certain voltage range – the range over which the transistor is biased in the appropriate region of operation (forward active for a BJT, saturation for a MOSFET). In general, we would normally like to have the largest possible voltage range for such a circuit to make the overall circuit as robust as possible. You may also notice that, unlike in Fig. 4.1(a) and (b), Figs. 4.1(c) and (d) include a ground symbol. It is normally the case that the emitter (or source) of an n-type transistor used as a current source is connected to ground in order to most easily provide the appropriate biasing. Thus another practical limitation is that such a current source realization is restricted to generating a current that is conducted from any arbitrary internal circuit node into ground. Here is a summary of these restrictions for current sources realized by n-type devices:

1. $I$ must be positive.

2. $V$ must be positive and restricted to a certain range sufficiently higher than zero. For a BJT implementation, the condition is $V > V_{CE(sat)}$; for a MOSFET implementation, the condition is $V > V_{GS} - V_t$.

3. Only the node into which the current is conducted can be arbitrarily specified; the other node (where the current comes out) must be a supply voltage or ground.

We will investigate p-type devices used to realize current sources shortly.

### 4.2 Biasing of Current Sources

You may have noticed that the implementation shown in Fig. 4.1(c) (resp. Fig. 4.1(d)) requires connecting a voltage source directly between the base and emitter of the BJT (resp. between the gate and source of the MOSFET). As discussed at length in the previous chapter, this is not practical because of the strong sensitivity of the collector current to PVT. One improvement that had been discussed previously is as shown in Fig. 4.2(a), where emitter
degeneration has been added. This will certainly make the operating point more robust, but there will also be a substantial voltage (much larger than $V_T$, as described in the previous chapter) across the resistor. Thus the minimum voltage $V$ is now increased by that IR drop; that is, the voltage range is now constrained to be:

$$V > V_{CE(sat)} + I_S R_E$$

For the MOSFET version shown in Fig. 4.2(b), the voltage range is given by:

$$V > (V_G - V_t) + I_S R_S$$

Thus we have a fundamental trade-off between the robustness of the operating point and the voltage range of the current source. (The output resistance for these current sources is substantially larger than $r_o$ as well; we will discuss this in more detail later in this chapter.)

### 4.2.1 Current Mirror

In an attempt to have a better trade-off—one that allows a robust operating point without the loss of voltage range—let us approach this problem in the reverse—that is, we will consider the behavior of a transistor that is known to be conducting a certain current, and understand how the appropriate $V_{BE}$ could be generated as a result. This concept is illustrated in Fig. 4.3(a), where it is assumed that an ideal current source is available. (We'll concern ourselves with where this ideal current source comes from shortly.) We have two voltages in this circuit: Voltage $V_{BE}$ must be very precisely set so that the BJT can conduct the collector current that is forced by current source $I_{REF}$. On the other hand, voltage $V_{CE}$ can be any voltage that is high enough so that the transistor is biased in the forward-active region.

Instead of applying an external voltage between the base and emitter, it would be desirable to somehow have the circuit bias itself. A very simple way to do this would be to just connect the collector and the base together, as shown in Fig. 4.3(b). To understand how this circuit would operate, let us think about how it would behave with $I_{REF}$ initially set to zero, so that the transistor is at first biased in the cutoff region with $V_{BE} = V_{CE} = 0$. We then imagine that $I_{REF}$ is stepped to its desired value at $t = 0$. How would the Fig. 4.3(b) respond? Any transistor will have some capacitance present between the base and emitter, and between the collector and substrate, as described in an earlier chapter. These capacitances are modeled in Fig. 4.3(b) as $C_x \equiv C_{BE} + C_{sub}$. (The exact value of this
Figure 4.2: (a) BJT current source with emitter degeneration; (b) MOSFET current source with source degeneration.
Figure 4.3: Evolution of a current mirror.
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Since the initial $V_{BE}$ is 0, then the initial collector current must also be zero and thus initially $I_{REF}$ must all be conducted in the capacitor, which causes $V_{BE}$ to increase from zero. As a result, $I_C$ will increase from zero as well. The circuit will reach equilibrium when $I_C + I_B = I_{REF}$, at which point there will no longer be any current charging the capacitance. At this equilibrium, the $V_{BE}$ will have attained exactly the right value that corresponds to the applied $I_{REF}$. Thus the circuit biases itself—that is, given the current, the circuit itself converges exactly to the correct $V_{BE}$. (Note that since we have forced $V_{BC} = 0$, this transistor must be biased in the forward-active region.)

Now that we have discovered a simple way of making the circuit generate just the right $V_{BE}$ that corresponds to a desired current $I_{REF}$, let us apply that same voltage to another transistor. This concept is shown in Fig. 4.3(c), where the two transistors $Q_A$ and $Q_B$ are assumed to have identical characteristics. (As discussed earlier, this is a very reasonable assumption when the two transistors are realized on the same substrate and are placed very close to each other with the same orientation.) These transistors are connected so that their respective bases and emitters are connected together; thus their base-emitter voltages are identical. If both transistors are biased in the forward-active region, then their collector currents must be almost exactly the same as well. Thus, we can conclude that $I_{OUT} \approx I_{REF}$. Since the action of this circuit is to replicate a current in one transistor (reference current $I_{REF}$) by a current in another transistor (output current $I_{OUT}$), we call this structure a current mirror.

We can now revisit the question of how the current source $I_{REF}$ is derived. In Fig. 4.3(c), we see that since this current source is connected between $V_{CC}$ and diode-connected transistor $Q_A$, the voltage across is well-defined and straightforward to calculate. Thus, we could easily generate the desired $I_{REF}$ simply by placing a resistor as shown in Fig. 4.3(d). From this circuit we can write:

$$I_{REF} = \frac{1}{R_{REF}} \cdot (V_{CC} - V_{BE}) \quad (4.1)$$

The exact same circuit topology can be used to realize a CMOS current mirror, shown in Fig. 4.3(e); the reference current can be calculated as:

$$I_{REF} = \frac{1}{R_{REF}} \cdot (V_{DD} - V_{GS}) \quad (4.2)$$

Unlike the BJT case, we can’t assume that $V_{GS}$ is some constant value. Normally for this current mirror, we try to estimate $V_{GS}$ using a hand calculation and then run a simulation for better accuracy.
To summarize, we have found a way to realize a robust current reference, whose value is nearly proportional to the supply voltage, and replicate this to another transistor. The voltage $V_{BE}$ or $V_{GS}$ is generated automatically from the reference branch; thus the circuit is self-biasing.

The current mirror is an especially flexible structure; we can arrange to have more than one current source derived from the same reference branch, and we can also arrange to have scaled versions. This is illustrated in the current mirror shown in Fig. 4.4, where all transistors are assumed to have identical $W/L$ ratios and characteristics. By the action of the current mirror, each individual transistor should conduct $I_{REF}$; thus, $I_{OUT1} = I_{REF}$, and $I_{OUT2} = 2I_{REF}$.

We can also use a p-type device to realize a current mirror. The BJT and MOSFET versions using pnp and p-channel transistors, respectively, are shown in Fig. 4.5(a) and (b). The operation of these current sources is identical to those in Fig. 4.1(d) and (e), respectively, except that the currents are conducted from the positive supply voltage into the output node.

### 4.3 Nonidealities in Current Sources

Although we wish to replicate, as closely as possible, $I_{OUT}$ with $I_{REF}$ in a current mirror, in reality these two currents will not be exactly the same. The difference between these two currents, which is defined as the error...
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![Diagrams of current mirrors](image-url)

Figure 4.5: (a) pnp current mirror; (b) PMOS current mirror.

current, comes from a number of different non-ideal effects, which will be explained in the following sections.

4.3.1 Effect of Transistor Finite Output Resistance

Let us consider the MOSFET current mirror shown in Fig. 4.6(a), where the two transistors are assumed to be identical. Because the two transistors have identical characteristics and have the same $V_{GS}$, they must share the same $I_D$ vs. $V_{DS}$ characteristic, shown in Fig. 4.6(b).

In general, a current source should conduct a constant current for any voltage within the specified range. However, from Fig. 4.6(b) we see that, due to the channel modulation effect in transistor $M_2$, the drain current has some dependence on the drain voltage. In particular, any difference between the drain voltages of transistors $M_1$ and $M_2$ will cause some mismatch between $I_{OUT}$ and $I_{REF}$. This is illustrated in Fig. 4.6(b), where it is indicated that the drain voltage of $M_1$ is fixed, due to the diode connection, at $V_{GS}$. From this figure we can derive the expression for the difference in currents as follows:

$$I_{OUT} - I_{REF} = \frac{1}{r_o}(V_{D2} - V_{GS})$$  \hspace{1cm} (4.3)

Expressing $r_o$ as $1/\lambda I_{REF}$, we can write (4.3) as:

$$I_{OUT} - I_{REF} = \lambda I_{REF} \cdot (V_{D2} - V_{GS})$$  \hspace{1cm} (4.4)
Figure 4.6: (a) MOS current mirror with $V_{D1} \neq V_{D2}$; (b) $I_D$ vs. $V_{DS}$ characteristic.

Defining $\Delta I \equiv I_{OUT} - I_{REF}$ and $\Delta V \equiv V_{D2} - V_{GS}$ as illustrated in Fig. 4.6(b), we can rewrite (4.4) as:

$$\frac{\Delta I}{I_{REF}} = \lambda \frac{\Delta V}{V_{A}}$$

A similar analysis (left as a homework problem) on a BJT current source yields a similar expression:

$$\frac{\Delta I}{I_{REF}} = \frac{\Delta V}{V_{A}}$$

(4.6)
Example 4.1:
In the MOSFET current mirror shown in Fig. 4.6(a), let \( V_{DD} = 1.8 \) V, \( V_i = 0.4 \) V, \( k' = 150 \) \( \mu A/V^2 \), and \( \lambda = 0.1 V^{-1} \). We wish to design this circuit so that \( I_{REF} = 200 \) \( \mu A \) and \( V_{GS} - V_i = 0.45 \) V. Find the values of \( R_{REF} \) and transistor \( W/L \). Then find \( I_{OUT} \) for \( V_{D2} = 0.85 \) V, \( 0.75 \) V, and \( 0.95 \) V.

We first find the transistor \( W/L \) that allows the transistor to conduct 200 \( \mu A \) with \( V_{GS} - V_i = 0.45 \) V:

\[
200 \ \mu A = \frac{150 \ \mu A/V^2 W}{2} \frac{W}{L} \left(0.45 V\right)^2
\]

\[
\Rightarrow \frac{W}{L} = 13.1
\]

Next we find the resistor value, observing that \( V_{GS} = 0.45 V + 0.4 V = 0.85 V \):

\[
200 \ \mu A = \frac{1}{R_{REF}} (1.8 V - 0.85 V)
\]

\[
\Rightarrow R_{REF} = 4.75 \text{ k\Omega}
\]

Now that we have designed the circuit so that \( I_{REF} = 200 \) \( \mu A \), let us consider \( I_{OUT} \). Notice that in our design we have set the value of \( V_{D1} = V_{GS1} = 0.85 V \). Thus any difference between \( V_{D1} \) and \( V_{D2} \) will give rise to a mismatch between \( I_{REF} \) and \( I_{OUT} \).

For \( V_{D2} = 0.85 \) V we have \( V_{D1} = V_{D2} \), thus \( I_{OUT} = 200 \) \( \mu A \) exactly.

For \( V_{D2} = 0.75 \) V we first need to verify that transistor \( M_2 \) is still biased in the saturation region. Since \( V_{GD2} = 0.85 \) V \( - 0.75 \) V \( < V_i \) this is indeed true. Since \( \Delta V = V_{D2} - V_{D1} = -0.1 \) V, we can write the following, based on (4.5):

\[
\frac{\Delta I}{I_{REF}} = \lambda \Delta V
\]

\[
= (0.1 \text{ V}^{-1})(-0.1 \text{ V}) = -0.01
\]

\[
\Rightarrow \Delta I = (200 \ \mu A)(-0.01) = -2 \ \mu A
\]

\[
\Rightarrow I_{OUT} = I_{REF} + \Delta I = 198 \ \mu A
\]

For \( V_{D2} = 0.95 \) V, it is obvious that transistor \( M_2 \) is biased in saturation since \( V_{DS2} > V_{DS1} \). For this case we have \( \Delta V = 0.1 \) V and we can calculate the following:

\[
\frac{\Delta I}{I_{REF}} = (0.1 \text{ V}^{-1})(0.1 \text{ V})
\]

\[
\Rightarrow \Delta I = (200 \ \mu A)(0.01) = 2 \ \mu A
\]

\[
\Rightarrow I_{OUT} = 202 \ \mu A
\]
Example 4.2:
In a BJT current mirror let $V_{CC} = 3.3$ V, $V_{BE(on)} = 0.65$ V, and $V_A = 75$ V.
We wish to design this circuit so that $I_{REF} = 500$ $\mu$A. Find the values of $R_{REF}$. Then find $I_{OUT}$ for $V_{C2} = 0.65$ V and 0.75 V.

We find the resistor value:

$$500 \mu A = \frac{1}{R_{REF}}(3.3 \text{ V} - 0.65 \text{ V})$$
$$\Rightarrow R_{REF} = 5.3 \text{ k}\Omega$$

Now that we have designed the circuit so that $I_{REF} = 200 \mu A$, let us consider $I_{OUT}$.
For $V_{C2} = 0.65$ V, we have $V_{C1} = V_{C2}$; thus $I_{OUT} = 500 \mu$A exactly.
For $V_{C2} = 0.75$ V, we have $\Delta V \equiv V_{C2} - V_{C1} = 0.1$ V, we can write the following, based on (4.6):

$$\frac{\Delta I}{I_{REF}} = \frac{\Delta V}{V_A}$$
$$= \frac{0.1 \text{ V}}{75 \text{ V}} = 0.0013$$
$$\Rightarrow \Delta I = (500 \mu A)(0.0013) = 0.67 \mu A$$
$$\Rightarrow I_{OUT} = I_{REF} + \Delta I = 501 \mu A$$

4.3.2 Effect of BJT Finite $\beta$

We now consider a non-ideality that is specific to BJT current sources. In our analyses so far, we have assumed that base currents in the transistors were negligible. We now consider how these finite base currents affect the operation of a current mirror.

The BJT current mirror shown in Fig. 4.7(a) has its base currents and collector currents labeled. For this analysis we assume that the transistors exhibit identical characteristics and that $r_o = \infty$. Under these conditions and given that the circuit topology forces the $V_{BE}$ of the two transistors to be the same, then the collector currents of the two transistors must be identical, and the base currents must also be identical. These are indicated in Fig. 4.7(a).

We can notice right away that current $I_{REF}$ must conduct current into
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Figure 4.7: BJT current mirror with multiple current sources.
the collector of \( Q_{1A} \) as well as the base currents of both transistors, while
current \( I_{OUT} \) is only the collector current of \( Q_{1B} \). This is essentially why
there will be an error between \( I_{OUT} \) and \( I_{REF} \). We begin our quantitative
analysis by writing a KCL equation at the diode-connected node, which
gives:
\[
I_{REF} = I_C + 2I_B
\]
(4.7)
Since \( I_B = I_C/\beta_F \), the above equation can be rewritten as:
\[
I_{REF} = I_C + 2\frac{I_C}{\beta_F}
= I_C \cdot \left(1 + \frac{2}{\beta_F}\right)
= I_{OUT} \cdot \left(1 + \frac{2}{\beta_F}\right)
\]
\[
\rightarrow I_{OUT} = \frac{I_{REF}}{1 + \frac{2}{\beta_F}}
\]
(4.8)
As in the previous analysis, we wish to find an expression for \( \Delta I \equiv I_{OUT} - I_{REF} \):
\[
\Delta I = I_{OUT} - I_{REF}
= I_{REF} \cdot \left[\frac{1}{1 + \frac{2}{\beta_F}} - 1\right]
= I_{REF} \cdot \frac{-\frac{2}{\beta_F}}{1 + \frac{2}{\beta_F}}
\]
\[
\rightarrow \frac{\Delta I}{I_{REF}} = -\frac{2}{1 + \frac{2}{\beta_F}}
\]
(4.9)
If we assume that \( 2/\beta_F \ll 1 \), then we can approximate the above as:
\[
\frac{\Delta I}{I_{REF}} \approx -\frac{2}{\beta_F}
\]
(4.10)
As mentioned previously, designers often use a single reference branch to
realize multiple current sources, as illustrated in Fig. 4.7(b). It is clear from
this figure that the base current error will increase from that illustrated in
Fig. 4.7(a); in particular, (4.10) is modified for this circuit to be:
\[
\frac{\Delta I}{I_{REF}} \approx -\frac{n + 1}{\beta_F}
\]
(4.11)
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assuming that \((n + 1)/\beta_F << 1\). However, if \(n\) becomes too large, then the above assumption may no longer hold, in which case the relative error is no longer small. In order to realize this type of circuit, it is necessary to improve the circuit in such a way as to decrease this error.

We now use a very common method to reduce error: We first amplify the error, then feed it back. This concept, realized as shown in Fig. 4.7(c), operates as follows for this circuit. The difference between the two currents, \(\Delta I \equiv I_{REF} - I_C\), is applied to the base of transistor \(Q_{err}\). The emitter current of this transistor is thus \((\beta_F + 1)\Delta I\), which is then applied to the bases of the other transistors. Since these transistor base currents are still on the order of \(I_C/\beta_F\), similar to the Fig. 4.7(b) circuit, the result is that \(\Delta I\) will be smaller by approximately a factor of \(\beta_F\). The quantitative analysis of the Fig. 4.7(c) circuit is almost identical to that of Fig. 4.7(b), except for the factor of \(\beta_F\) reduction in \(\Delta I\). Thus by modifying the equations given above, we can write for this circuit the following:

\[
I_{REF} = I_C + \frac{n + 1}{\beta_F + 1} \cdot I_B
\]

\[
= I_C + \frac{n + 1}{\beta_F} \cdot \frac{I_C}{\beta_F}
\]

\[
= I_{OUT} \cdot \left[1 + \frac{n + 1}{\beta_F(\beta_F + 1)}\right]
\]

\[
\rightarrow I_{OUT} = \frac{I_{REF}}{1 + \frac{n + 1}{\beta_F(\beta_F + 1)}}
\]

(4.12)

(4.13)

We now solve for \(\Delta I\) as before:

\[
\Delta I \equiv I_{OUT} - I_{REF}
\]

\[
= I_{REF} \cdot \frac{n + 1}{\beta_F(\beta_F + 1)}
\]

\[
\rightarrow \frac{\Delta I}{I_{REF}} = -\frac{n + 1}{\beta_F(\beta_F + 1)} \cdot \frac{n + 1}{\beta_F(\beta_F + 1)}
\]

(4.14)

If we now assume, as before, that \(\beta_F >> 1\) and that \((n + 1)/\beta_F^2 << 1\) (notice that this is much more easily satisfied when the transistor \(\beta\) is now squared), the above can be approximated as:

\[
\frac{\Delta I}{I_{REF}} \approx -\frac{n + 1}{\beta_F^2}
\]

(4.15)
Thus the inclusion of transistor $Q_{err}$ effectively reduces the error by a factor of $\beta_F$.

Note that the expression for $I_{REF}$ is somewhat different in this current mirror than for the simple version because of the additional $V_{BE}$ drop in transistor $Q_e$. In particular, we can write:

$$I_{REF} = \frac{1}{R_{REF}} (V_{CC} - 2V_{BE})$$

(4.16)

Since MOSFETs do not conduct any appreciable gate current, the Fig. 4.7(c) circuit topology is generally only useful for BJT circuits, not for MOSFET circuits.

### 4.3.3 Effect of Random Transistor Mismatches

The operation of a current mirror is based on the assumption that the pair of transistors is identical in size and electrical parameters and hence perfectly matched. In reality, there is always some small statistical variation between the parameters in any pair of devices, which will give rise to small mismatches in $I_{REF}$ and $I_{OUT}$. Details of how these variations arise will be given in a later chapter. For now we will consider how these variations affect the current mirror accuracy.

For the MOSFET current mirror in Fig. 4.3(e), suppose that there is a small mismatch in $k'$ between the transistors, $\Delta k'$, so that we have the following equations:

$$I_{REF} = \frac{k' W}{2 L} (V_{GS} - V_t)^2$$

$$I_{OUT} = \frac{k' + \Delta k'}{2} \frac{W}{L} (V_{GS} - V_t)^2$$

This gives:

$$\frac{I_{OUT}}{I_{REF}} = 1 + \frac{\Delta k'}{k'}$$

$$\frac{\Delta I}{I_{REF}} = \frac{\Delta k'}{k'}$$

As expected, a percentage mismatch in $k'$ results in an identical percentage mismatch in $\Delta I$.

For the same MOSFET current mirror, suppose now that there is a small mismatch in $V_t$ between the transistors, $\Delta V_t$, so that we have the following
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\[ I_{REF} = \frac{k' W}{2 L} [V_{GS} - V_t] \]

\[ I_{OUT} = \frac{k' W}{2 L} [V_{GS} - (V_t + \Delta V_t)]^2 \]

\[ = \frac{k' W}{2 L} (V_{GS} - V_t)^2 \left[ 1 - \left( \frac{\Delta V_t}{V_{GS} - V_t} \right)^2 \right] \]

This gives:

\[ \frac{I_{OUT}}{I_{REF}} = \left[ 1 - \left( \frac{\Delta V_t}{V_{GS} - V_t} \right)^2 \right] \]

\[ \rightarrow \frac{\Delta I}{I_{REF}} = -2 \frac{\Delta V_t}{V_{GS} - V_t} + \left( \frac{\Delta V_t}{V_{GS} - V_t} \right)^2 \]

If \( \Delta V_t \ll V_{GS} - V_t \), the above expression can be approximated as:

\[ \frac{\Delta I}{I_{REF}} \approx -2 \frac{\Delta V_t}{V_{GS} - V_t} \]

Note that the value of \( V_{GS} - V_t \) that we set in the design has a significant impact on the current mismatch due to this effect. Similar calculations can be done for the BJT current mirror shown in Fig. 4.3(d); these have been left as a homework problem.

4.4 Current Sources with High Output Resistance

4.4.1 Source Degeneration of MOSFET Current Mirror

There may be occasions where the output resistance needs to be higher than a transistor \( r_o \). (As we will see in the next chapter, this is particularly important when a very high voltage gain is desired.) In order to increase the output resistance we might consider modifying a current mirror to include a degeneration resistance, shown in the degenerated MOSFET current mirror in Fig. 4.8(a).

Since degeneration resistor \( R_S \) is connected in series with the source of transistor \( M_1 \), at first glance we might guess that the resulting output resistance of the Fig. 4.8(a) current source would simply \( r_o + R_S \). In fact, the situation is more complex. To analyze the output resistance, we construct the small-signal diagram shown in Fig. 4.8(b), where as usual we apply a small-signal voltage \( v_x \) to the output and measure the resulting small-signal
Figure 4.8: (a) MOS current mirror with resistor degeneration; (b) small-signal schematic; (c) simplified schematic; (d) MOS cascode current mirror; (e) simplified schematic; (f) cascode current mirror showing dc voltages.
current $i_x$. Note that since transistor $M_{1A}$ diode-connected, its small-signal equivalent is simply a resistor with value $\frac{1}{g_{m1}}|v'_{o1}|$.

Before analyzing the circuit further, we can make an important observation: The left-hand side of the Fig. 4.8(b) circuit has no connection to any small-signal sources; therefore all three resistors on the left side must conduct zero current and small-signal voltage $v_{g1}$ must be zero. (Note however that small-signal voltage $v_{g1B}$ is not zero — as we will see, this fact has a very important effect on the output resistance.) Thus we can simplify the circuit by replacing those three resistors with a small-signal ground as shown in Fig. 4.8(c). In other words, this simplification reflects the fact that any change in the output voltage will have no effect on $I_{REF}$ and on $V_{G1}$. We have made another change in Fig. 4.8(c): Instead of drawing the entire small-signal schematic equivalent of transistor $M_{1B}$, we are showing the transistor symbol with its $r_o$ explicitly displayed. Thus in the context of a small-signal analysis the transistor symbol represents primarily its small-signal transconductance. We will be using this symbology often from now on because the circuit schematics are easier to read and it brings more intuition into the analysis.

To analyze the Fig. 4.8(c) circuit, we first write the KCL equation at the output node:

$$i_x = g_{m1}v_{g1B} + \frac{v_x - v_s}{r_{o1}}$$

(4.17)

where $v_s$ is the small-signal voltage at the transistor source node. We now make a simplifying observation: the small-signal current $i_x$ conducted into the transistor drain must be identical to the small-signal current conducted out of the transistor source, regardless of how this current splits between $r_{o1}$ and the dependent current source within the transistor. Thus we can write:

$$v_s = i_x R_S$$

$$\rightarrow v_{g1B} = -i_x R_S$$

Substituting these identities back into (4.17), we have:

$$i_x = -g_{m1}i_x R_S + \frac{1}{r_{o1}}(v_x - i_x R_S)$$

(4.18)

$$\rightarrow i_x \left(1 + g_{m1} R_S + \frac{R_S}{r_{o1}}\right) = \frac{v_x}{r_{o1}}$$

(4.19)

Solving the above equation for $v_x/i_x$, we have:

$$\frac{v_x}{i_x} \equiv r_{out} = r_{o1} \left(1 + g_{m1} R_S + \frac{R_S}{r_{o1}}\right)$$

$$= R_S + r_{o1}(1 + g_{m1} R_S)$$

(4.20)
Note that the expression in (4.20) expresses $R_S$ in series with another resistance, but that other resistance is actually much larger than the transistor $r_o$! To understand this expression better, let us first examine the $g_{m1}R_S$ term:

$$g_{m1}R_S = \frac{2I_D R_S}{V_{GS1} - V_t}$$

As mentioned previously, it is desirable to have this expression much larger than unity, and thus we would design the circuit so that the voltage drop across $R_S$ is much larger than $V_{GS} - V_t$. Thus we can approximate (4.20) as:

$$r_{out} = R_S + r_o g_{m1} R_S = R_S(1 + g_{m1} r_o)$$

Furthermore, since in general $g_m r_o >> 1$, we have:

$$r_{out} \approx g_{m1} r_o R_S$$

$$= R_S \cdot \frac{2 I_D}{V_{GS1} - V_t} \cdot \frac{1}{\lambda I_D}$$

$$= R_S \cdot \frac{2}{\lambda (V_{GS1} - V_t)}$$ \hspace{1cm} (4.21)

As mentioned earlier, note that the IR drop across $R_S$ will limit the headroom for the output voltage.
Example 4.3:
We wish to design a MOSFET current source with source degeneration that conducts 250 \( \mu \text{A} \) and has \( r_{\text{out}} \geq 100 \text{ k}\Omega \) while having a voltage drop of no more than 0.75 V across \( R_S \). Then find the output voltage range for which this current mirror maintains its high \( r_{\text{out}} \). Assume \( \lambda = 0.15 \text{ V}^{-1} \), \( k' = 100 \mu \text{A}/\text{V}^2 \), \( V_t = 0.4 \text{ V} \), and \( V_{DD} = 1.8 \text{ V} \).

We begin by considering the constraint on the voltage drop across \( R_S \). We can write:

\[
0.75 \text{ V} \geq (250 \mu \text{A})(R_S) \\
\rightarrow R_S \leq 3 \text{ k}\Omega
\]

Since we are trying to maximize \( r_{\text{out}} \), we will choose this maximum value of \( R_S = 3 \text{ k}\Omega \).

Now using the approximation in (4.21), all that is left is to solve for \( V_{GS1} - V_t \):

\[
100 \text{ k}\Omega \leq (3 \text{ k}\Omega) \cdot \frac{2}{(0.15 \text{ V}^{-1})(V_{GS1} - V_t)} \\
\rightarrow V_{GS1} - V_t \leq 400 \text{ mV}
\]

We will choose \( V_{GS} - V_t = 400 \text{ mV} \), which gives \( V_{GS1} = 800 \text{ mV} \).

We now proceed with the remainder of the design: Given \( I_D R_S = 0.75 \text{ V} \) and \( V_{GS1} = 0.8 \text{ V} \), the voltage drop across \( R_{REF} \) must be 0.25 V, and thus \( R_{REF} = 0.25 \text{ V}/250 \mu \text{A} = 1.0 \text{ k}\Omega \). Finally, to find the transistor \( W/L \), we use:

\[
250 \mu \text{A} = \frac{100 \mu \text{A}/\text{V}^2}{2} \cdot \frac{W}{L} \cdot (0.4 \text{ V})^2 \\
\rightarrow \frac{W}{L} = 15.6
\]

The design is now complete.

To obtain a more precise value of \( r_{\text{out}} \), let us derive the small-signal parameters and apply them to (4.20):

\[
gm1 = \frac{(2)(250 \mu \text{A})}{0.4 \text{ V}} = 1.25 \text{ mS} \\
r_{o1} = \frac{1}{(0.15 \text{ V}^{-1})(250 \mu \text{A})} = 26.7 \text{ k}\Omega \\
\rightarrow r_{\text{out}} = 3 \text{ k}\Omega + 26.7 \text{ k}\Omega [1 + (1.25 \text{ mS})(3 \text{ k}\Omega)] \\
\quad = 3 \text{ k}\Omega + 26.7 \text{ k}\Omega (1 + 3.75) \\
\quad = 3 \text{ k}\Omega + 127 \text{ k}\Omega = 130 \text{ k}\Omega
\]
To find the output voltage range for which transistor $M_{1B}$ remains in saturation, we first find the gate voltage:

$$V_G = I_D R_S + V_{GS}$$
$$= 0.75 \text{ V} + 0.8 \text{ V} = 1.55 \text{ V}$$

Thus the minimum output voltage is given by:

$$V_{OUT\text{[min]}} = V_G - V_t$$
$$= 1.55 \text{ V} - 0.4 \text{ V} = 1.15 \text{ V}$$

We see from this example that the source degeneration results in a substantial increase in $r_{out}$, but the 0.75 V drop across $R_S$ causes a severe limitation in the output swing.

### 4.4.2 Cascode MOSFET Current Mirror

The above example illustrated a trade-off that we have seen before: The degeneration resistance gives a substantial increase in $r_{out}$, but at the expense of a reduced output swing. And once again, this is due to the fact that $R_S$ must simultaneously conduct both dc and small-signal current. In the case of the differential amplifier, we found that by replacing the load resistor with a transistor helped resolve this tradeoff. We can try this with the MOSFET current by using the structure shown in Fig. 4.8(d), where the degeneration resistors have been replaced by transistors $M_{2A}$ and $M_{2B}$. The resulting structure is known as a cascode configuration. (This word is a contraction from name of a technique, developed in the 1930’s on tube amplifiers, called “cascade to cathode.”)

We first qualitatively describe this circuit’s operation. Transistors $M_{2A}$ and $M_{2B}$ function as a conventional current mirror, thus setting $I_{OUT} = I_{REF}$ as long as they are well-matched. To determine this circuit’s small-signal output resistance, we make the same observation as for the Fig. 4.8(b) circuit that both gate voltages must act as small-signal grounds. Thus we can analyze the simplified circuit shown in Fig. 4.8(e). Furthermore, we can see by inspection in this circuit that small-signal voltage $v_{g2B}$ must be zero, since both the gate and source nodes are connected to small-signal ground. Thus the output resistance of this circuit is identical to that found for the Fig. 4.8(c) circuit, expressed in (4.20), but with $R_S$ replaced with $r_{o2}$:

$$\frac{v_x}{i_x} \equiv r_{out} = r_{o2} + r_{o1}(1 + g_m r_{o2})$$  \hspace{1cm} (4.22)
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If all transistors are the same length, thereby having the same $\lambda$, then we have $r_{o1} = r_{o2}$ and we can simplify (4.22) as:

\[
\begin{align*}
    r_{out} &= 2r_{o1,2} + g_m r_{o1,2}^2 \\
    &= r_{o1,2}(2 + g_m r_{o1,2}) 
\end{align*}
\] (4.23)

If we assume, as usual, that $g_m r_{o1,2} \gg 2$, then we can simplify this expression as:

\[
r_{out} \approx g_m r_{o1,2}^2
\] (4.24)

In other words, the cascode configuration increases the output resistance by a factor of $g_m r_o$.

To determine the output voltage range of the cascode current mirror, we consider the dc voltages at the gate nodes, shown in blue in Fig. 4.8(f): At the gates of transistors $M_{2A}$ and $M_{2B}$, we have $V_{GS} = V_l + \Delta V$, where $V_l$ is the threshold voltage and $\Delta V$ is the additional voltage needed to conduct the current, and is dependent on the value of $I_{REF}$ chosen, and the transistor parameters. Since $M_{2A}$ and $M_{2A}$ are connected in series, the voltage at the gates of transistors $M_{1A}$ and $M_{1B}$ will be (assuming that the transistors are all identical and body effect is ignored):

\[
2V_{GS} = 2V_l + 2\Delta V
\]

Therefore the minimum output voltage required to keep $M_{1B}$ in saturation must be one $V_l$ lower than the gate voltage of $M_{1B}$:

\[
V_{OUT\{min\}} = V_l + 2\Delta V
\] (4.25)

We can see that, unlike the Fig. 4.8(b) current mirror, there are no limitations from IR drops, and we can arrange to have $\Delta V$ made reasonably small. In addition, note that the drain voltages of $M_{1B}$ and $M_{2B}$ are the same, thereby maintaining very close matching of their currents. However, the $V_l$ term is fixed and still imposes an undesirable limitation on the swing.
Example 4.4:
Modify the current mirror designed in Example 4.3 into a cascode current mirror with all transistors having the same \( W/L \) ratios. Find the resulting \( r_{out} \) and minimum \( V_{OUT} \).

Referring to the schematic of the cascode current mirror shown in Fig. 4.8(f), we can use the expression for this circuit's output resistance in (4.22):

\[
r_{out} = r_{o2} + r_{o1}(1 + g_{m1}r_{o2})
\]

From the calculations down in Example 4.3, we have:

\[
r_{o1} = r_{o2} = 26.7 \text{ k\( \Omega \)} \quad g_{m1} = 1.25 \text{ mS}
\]

Plugging these values into the expression for \( r_{out} \), we have:

\[
\begin{align*}
    r_{out} &= 26.7 \text{ k\( \Omega \)} + 26.7 \text{ k\( \Omega \)} [1 + (1.25 \text{ mS})(26.7 \text{ k\( \Omega \)})] \\
          &= 26.7 \text{ k\( \Omega \)} + 26.7 \text{ k\( \Omega \)} [1 + 33.4] \\
          &= 26.7 \text{ k\( \Omega \)} + 918 \text{ k\( \Omega \)} \\
          &= 945 \text{ k\( \Omega \)}
\end{align*}
\]

To determine the output swing, we use the expression in (4.25) with, from the Example 4.3 design, \( V_i = 0.4 \text{ V} \) and \( \Delta V = 0.4 \text{ V} \), which gives:

\[
V_{OUT(min)} = 0.4 \text{ V} + (2)(0.4 \text{ V}) = 1.2 \text{ V}
\]

We see that \( r_{out} \) of the cascode configuration is over 7 times larger than that of the degenerated current mirror in Example 4.3, and over 35 times larger than that of a simple current mirror! Unfortunately the output swing is even worse in this configuration, due primarily to the fact that this swing is limited by the transistor \( V_i \).

How might we modify this circuit so that it retains its high \( r_{out} \) while further relaxing the voltage swing limitation? We begin by observing that the voltage at the drain of \( M_{2B} \) is also \( V_i + \Delta V \), which is the same as the voltage on its gate. Thus this transistor is certainly biased in the saturation region. In fact, we have some extra margin in the drain voltage that we can exploit. We could lower the drain voltage of \( M_{2B} \) by as much as a threshold voltage while still keeping this transistor in the saturation region. A simple idea for doing this is illustrated in Fig. 4.9(a). By decreasing the voltage on the gate of \( M_{1B} \) by \( V_i \), all transistors are still maintained in saturation (with \( M_{2B} \) now at the edge of saturation), and \( V_{OUT} \) can now go as low
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as $2\Delta V$, whose value can be chosen by the designer. Hence, there are two practical problems with this circuit. First, implementing a floating voltage source is impractical, so a more realistic way is needed to implement this voltage shift. Second, there is now a voltage difference of $V_t$ between the drains of transistors $M_{2A}$ and $M_{2B}$, causing a substantial mismatch between $I_{REF}$ and $I_{OUT}$.

This circuit can be improved by removing the diode connection in transistor $M_{1A}$ and applying the voltage source to the gates of both $M_{1A}$ and $M_{1B}$ as shown in Fig. 4.9(b). We also remove the diode connection in transistor $M_{2A}$ and instead connect its gate to the $M_{1A}$ drain. Although this connection looks quite different from the standard diode-connected transistors, in fact all of the transistors are still biased in the saturation region, and the drain voltages of $M_{2A}$ and $M_{2B}$ are both now $\Delta V$, thereby restoring the very accurate matching of the two currents.

We complete this design by realizing the grounded voltage source. Since the voltage that we are trying to realize, $V_t + 2\Delta V$, includes a single $V_t$, this could be most directly realized by a single $V_{GS}$ of an n-channel MOSFET. This is shown in Fig. 4.9(c) as diode-connected transistor $M_3$ biased by a simple resistor connected to $V_{DD}$. Because $V_{GS3}$ should be different from the $V_{GS}$ of the other transistors in this circuit, we need to design the appropriate current $I_3$ and sizing $(W/L)_3$. To realize the $2\Delta V$ component of $V_{GS3}$, we should arrange this transistor to have a current density (that is, the current per unit width) to be four times that of the other transistors in the circuit. This is because, due to the square-law behavior of MOSFETs, if the transistor’s $V_{GS} - V_t$ is increased by a factor of 2, then the current must increase by a factor of 4. There are two ways that this could be done: We could arrange to have $(W/L)_3 = (W/L)_2$ and thus set $I_3 = 4I_{REF}$, or we could arrange to have $I_3 = I_{REF}$ and thus set $(W/L)_3 = \frac{1}{4}(W/L)_2$. Normally the latter arrangement is selected, simply because it requires less dc current in $M_3$, thereby requiring slightly smaller power dissipation.
Figure 4.9: (a) Illustration of how level shifting could increase output swing; (b) Modified version with grounded voltage source; (c) Modified version with better matching in current mirror; (c) Final version of wide-swing cascode.
Example 4.5:
Modify the cascode current mirror designed in Example 4.4 into a wide-swing version. Find the resulting $r_{out}$ and minimum $V_{OUT}$.

Referring to the schematic of the cascode current mirror shown in Fig. 4.9(c), the $W/L$ ratio of transistors $M_{1A}, M_{1B}, M_{2A}$, and $M_{2B}$ of 15.6 stay the same as in Example 4.4. All that is left to do is find the values of $R_{REF} R_3$, and $(W/L)_3$.

Note that while the voltage across $R_{REF}$ in Fig. 4.8(f) is $V_{DD} - 2V_{GS}$, that voltage in Fig. 4.9(c) is $V_{DD} - V_{GS}$. Thus we can write:

$$I_{REF} = \frac{1}{R_{REF}} (V_{DD} - V_{GS})$$

$$\rightarrow R_{REF} = \frac{V_{DD} - V_{GS}}{I_{REF}}$$

$$= \frac{1.8 \text{ V} - 0.8 \text{ V}}{250 \mu\text{A}} = 4 \text{ k}\Omega$$

As discussed earlier, we arrange to have $(W/L)_3$ to be 4 times smaller than the other transistors in order to achieve a voltage of $V_l + 2\Delta V = 1.2 \text{ V}$; thus $(W/L)_3 = 3.9$. We also arrange $I_3 = I_{REF} = 250 \mu\text{A}$. Thus we can write:

$$I_3 = \frac{1}{R_3} (V_{DD} - V_{GS})$$

$$\rightarrow R_3 = \frac{V_{DD} - V_{GS}}{I_3}$$

$$= \frac{1.8 \text{ V} - 1.2 \text{ V}}{250 \mu\text{A}} = 2.4 \text{ k}\Omega$$

As described earlier, the output voltage can swing as low as $2\Delta V$ while keeping all transistors in the saturation region. Thus we have:

$$V_{OUT(min)} = 0.8 \text{ V}$$

Note that this is a substantially improved swing over the cascode current mirror designed in Example 4.4. Moreover, since the expression does not include $V_t$, the designer can arrange to make the output swing even closer to ground by reducing $\Delta V$ (which can be adjusted by increasing the $W/L$ of the transistors).
4.4.3 BJT Current Mirror with Emitter Degeneration

Degeneration can also be used in a BJT current mirror, as shown in Fig. 4.10(a). The corresponding small-signal schematic shown in Fig. 4.10(b), where \( r_{e1} \) is the small-signal equivalent resistance of diode-connected transistor \( Q_{1A} \). Unlike the MOSFET case, since the small-signal base current of \( Q_{1B} \) is not zero, we can no longer assume that the small-signal base voltage of transistors \( Q_{1A} \) and \( Q_{1B} \) is zero. Thus in the circuit to be analyzed in Fig. 4.10(c), we must include the equivalent resistance \( R_{eq} \) between the base node and ground in our calculations. This additional effect, not seen in a MOSFET current mirror, will prove to make the analysis more complicated than for the MOSFET case. To better understand this effect, we will first observe in Fig. 4.10(c) that if the current conducted in the base of \( M_{1B} \) is \( i_b \), then by KCL the current conducted from the emitter of \( M_{1B} \) must be \( i_b + i_x \), as illustrated in this figure. We can determine the relationship between \( i_b \) and \( i_x \) by writing a KVL equation around the loop consisting of voltage drops across \( R_{eq}, r_{\pi 1B} \), and \( R_E \):

\[
i_b R_{eq} + i_b r_{\pi 1B} + (i_b + i_x) R_E = 0 \quad (4.26)
\]

\[
\rightarrow i_b = \frac{R_E}{i_x R_E + R_{eq} + r_{\pi 1B}} \quad (4.27)
\]

\[
\approx \begin{cases} 
  -i_x \frac{R_E}{r_{\pi 1B}}, & r_{\pi 1B} >> R_E + R_{eq} \\
  -i_x \frac{R_E}{R_E + R_{eq}}, & r_{\pi 1B} << R_E + R_{eq}
\end{cases} \quad (4.28)
\]

To develop some intuition for this circuit, we will first consider two extreme cases: We see from the above equation that for \( R_E + R_{eq} \) very small, \( i_b \) will be small as well; thus the effect will be similar to the MOSFET case; that is, we would expect to have:

\[
r_{out} \approx r_{o1} + R_E + g_m R_E r_{o1} \quad (4.29)
\]

\[
\approx g_m R_E r_{o1}
\]

However, for \( R_E \) very large, (4.28) gives \( i_b \approx i_x \). This can be seen by considering the extreme case where \( R_E \) is replaced by an open circuit, as illustrated in Fig. 4.10(d). In this case it is clear that by KCL, \( i_b = -i_x \). Taking this further, we can also see that the emitter current must be \((\beta + 1)i_b\), and this current must also be conducted back through \( r_{o1} \), as illustrated in Fig. 4.10(d). Thus writing a KVL equation consisting of voltage drops across \( R_{eq}, r_{\pi 1B} \), and \( r_{o1} \), we have:

\[
i_b R_{eq} + i_b r_{\pi 1B} + (\beta + 1)i_b r_{o1} + v_x = 0
\]
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Figure 4.10: (a) BJT current mirror with emitter degeneration;
which gives:

\[ r_{out} = -\frac{v_x}{i_x} = R_{eq} + r_{\pi 1B} + (\beta + 1)r_{o1} \quad (4.30) \]

\( \approx \beta r_{o1} \)

If we compare (4.29), we see that for high values of \( R_E \), the expression \( g_{m1}R_E \) is replaced by \( \beta \) for the BJT current mirror. (We will see shortly that a more exact analysis of this expression gives approximately half the value derived above.)

Now that we have some intuition into the behavior of this current mirror, we can do a more exact analysis. We begin by writing a KCL equation at the output node for Fig. 4.10(c):

\[ i_x = \frac{1}{r_{o1}} \left( v_x - v_e \right) + g_{m1}v_{\pi 1} \quad (4.31) \]

We can also write the following expressions for the voltages \( v_e \) and \( v_{\pi 1} \):

\[ v_e = R_E(i_b + i_x) \]

\[ v_{\pi 1} = -i_b R_{eq} - R_E(i_b + i_x) \]

Substituting the above expressions into (4.31), we have:

\[ i_x = \frac{1}{r_{o1}} \left[ v_x - R_E(i_b + i_x) \right] - g_{m1} \left[ R_{eq}i_b + R_E(i_b + i_x) \right] \]

Multiplying both sides by \( r_{o1} \) and gathering like terms together, we have:

\[ v_x = i_x r_{o1} \left[ R_E + g_{m1}r_{o1}R_E \right] + i_b \left[ R_E + g_{m1}r_{o1}(R_E + R_{eq}) \right] \]

Substituting (4.27) into the above expression, we have:

\[ v_x = i_x r_{o1} \left[ R_E + g_{m1}r_{o1}R_E \right] - i_x R_E \cdot \frac{R_E + g_{m1}r_{o1}(R_E + R_{eq})}{R_E + R_{eq} + r_{\pi 1}} \]

which gives:

\[ r_{out} = r_{o1} + R_E + g_{m1}R_Er_{o1} - R_E \cdot \frac{R_E + g_{m1}r_{o1}(R_E + R_{eq})}{R_E + R_{eq} + r_{\pi 1}} \]

Note that the first three terms on the right-hand side of the above expression are identical in form to that of the MOSFET degenerated current mirror;
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the second term, which subtracts from the first, will be significant only for sufficiently large values of $R_E$. This equation can be rearranged as follows:

$$r_{\text{out}} = r_{o1} + R_E \cdot \frac{R_{eq} + r_{\pi 1}}{R_E + R_{eq} + r_{\pi 1}} + R_E g_m r_{o1} \cdot \frac{r_{\pi 1}}{R_E + R_{eq} + r_{\pi 1}}$$

As done earlier, we will now consider two cases, depending on the relative value of $r_{\pi 1}$:

$$r_{\text{out}} \approx \begin{cases} 
  r_{o1} + R_E + g_m r_{o1} R_E, & r_{\pi 1} \gg R_E + R_{eq} \\
  r_{o1} + R_E || R_{eq} + \beta r_{o1} \cdot \frac{R_E}{R_E + R_{eq}}, & r_{\pi 1} \ll R_E + R_{eq}
\end{cases} \quad (4.32)$$

We now observe from Fig. 4.10(b) that $R_{eq}$ can be expressed as:

$$R_{eq} = R_{\text{REF}} || (r_{e1} + R_E) \quad (4.33)$$

It is often the case that $R_{\text{REF}} > R_E >> r_e$, and thus we can make the approximation:

$$R_{eq} \approx R_E$$

Applying the above approximation into (4.32) and assuming $\beta >> 1$, $g_m R_E >> 1$, and $r_{o1} >> R_E$, we can write:

$$r_{\text{out}} \approx \begin{cases} 
  r_{o1} \cdot (g_m R_E), & r_{\pi 1} \gg 2R_E \\
  r_{o1} \cdot \frac{\beta}{2}, & r_{\pi 1} \ll 2R_E
\end{cases} \quad (4.34)$$

In other words, for $g_m R_E << \beta/2$, the expression is similar to that from the source-degenerated MOSFET current mirror. For $g_m R_E >> \beta/2$, the expression no longer increases with $g_m R_E$.

As in the MOSFET case, we can imagine once again that the largest possible effective emitter degeneration resistance could be realized with the $r_o$ of another BJT, and thus construct the cascode configuration shown in Fig. 4.10(e). At first glance, it looks reasonable to use the expression in (4.34), substitute $R_E$ by $r_{o2}$, and conclude that $r_{\text{out}} \approx \beta r_{o2}/2$. Although this approach works for the MOSFET cascode, there is an additional effect in the BJT cascode that needs to be considered. Observing once again at the schematic in Fig. 4.10(e), any small-signal current $i_b$ conducted into the base of $Q_{1B}$ must be conducted from the impedance of $R_{\text{REF}}$ in parallel with the small-signal resistance of $Q_{1A}$ and $Q_{1B}$ as illustrated in Fig. 4.10(f). The portion of this small-signal base current that is conducted from the transistors, $a_i b$, is mirrored back to the collector current of $Q_{2B}$; this effect is modeled by the dependent current source in Fig. 4.10(f). To see how this
affects the small-signal operation, we first write the KVL equation, similar to (4.30), around the loop consisting of \( R_{e1}, r_{\pi 1B}, \) and \( r_{o2} \):

\[ a_i b (r_{e1} + r_{e2}) + i_b r_{\pi 1} + i_x + (1+a) b |r_{o2} = 0 \rightarrow i_b = \frac{r_{o2}}{a(r_{e1} + r_{e2}) + r_{\pi 1}(a + 1)r_{o2}} i_x \]

Assuming \( r_{o2} \) dominates the denominator of the above expression, we can simplify it as:

\[ i_b \approx -\frac{i_x}{a + 1} \]

Furthermore, we have the following expression for \( a \) from the action of the current division:

\[ a = \frac{R_{REF}}{R_{REF} + r_{e1} + r_{e2}} \approx 1 \]

and thus \( i_b \approx -i_x/2 \). Using this approximation, we have the current conducted through \( r_{o2} \) is \( i_x/2 \), and the current conducted upward through \( r_{o1} \) is \((\beta+1)i_b - (i_x + i_b) = -(\beta/2 + 1)i_x\). Thus we have:

\[ v_x = \left(\frac{\beta}{2} + 1\right) i_x r_{o1} + \frac{i_x}{2} r_{o2} \]

\[ \rightarrow r_{out} = \left(\frac{\beta}{2} + 1\right) r_{o1} + r_{o2} \approx \frac{\beta}{2} r_{o1} \]

This the same result as for case of emitter degeneration with a resistor, but for a somewhat different reason.

**Effect of Finite \( \beta \) in BJT Cascode**

As discussed in Section 4.3.2, the finite \( \beta \) of a BJT can affect the accuracy of a current mirror, and this is true for cascode structures as well. To understand this better, let us consider the dc currents in a BJT cascode, which are labeled in blue in Fig. 4.11(a). To understand why there is a difference between \( I_{OUT} \) and \( I_{REF} \), we consider the dc currents in the transistors: Current \( I_{REF} \) enters the diode-connected transistor \( Q_{1A} \), from which a small amount of current \( (I_{OUT}/\beta) \) is subtracted; the remainder of the current, \( I_{REF} - I_{OUT}/\beta \), is then conducted into diode-connected transistor \( Q_{2A} \). Turning out attention to the right-hand side of this schematic, we can also observe that the collector current of \( Q_{2B} \) must be the sum of the base and collector currents of \( Q_{1B} \), which is \( I_{OUT}(1 + 1/\beta) \). Since transistors \( Q_{2A} \) and \( Q_{2B} \) form a current mirror, their collector currents must
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![Diagram](image)

**Figure 4.11:** (a) BJT cascode with dc currents labeled; (b) Variation on BJT cascode.
be the same, and their base currents must be \( \beta \) times less than this value. As indicated in Fig. 4.11(a), the sum of the base currents of \( Q_{2A} \) and \( Q_{2B} \) must be \( \frac{2I_{OUT}}{\beta}(1 + \frac{1}{\beta}) \). To complete this analysis, we can now write a KCL equation at the emitter of \( Q_{1A} \):

\[
I_{E1A} = I_{C2A} + 2I_{B2} 
\rightarrow I_{REF} - \frac{I_{OUT}}{\beta} = I_{OUT} \left( 1 + \frac{1}{\beta} \right) + \frac{2I_{OUT}}{\beta} \left( 1 + \frac{1}{\beta} \right)
\]

Solving the above equation, we have:

\[
\frac{I_{OUT}}{I_{REF}} = \frac{1}{1 + \frac{1}{\beta} + \frac{2}{\beta^2}}
\]

Setting \( \Delta I \equiv I_{OUT} - I_{REF} \), we can write:

\[
\frac{\Delta I}{I_{REF}} = -\frac{\frac{4}{\beta} + \frac{2}{\beta^2}}{1 + \frac{1}{\beta} + \frac{2}{\beta^2}}
\]

Assuming that \( \beta \) is very large, we can retain just the dominant term in the numerator and denominator of the above expression, which gives:

\[
\frac{I_{OUT}}{I_{REF}} \approx \frac{-4}{\beta} \tag{4.35}
\]

If we compare the above expression with (4.10), we see that the Fig. 4.11(a) configuration has an even worse effect due to finite \( \beta \) than the standard current mirror! We can understand this qualitatively by observing that this circuit has two diode connections, both on the left-hand side, and thus there are two places were \( I_{REF} \) is reduced before it reaches the current mirror realized by \( Q_{2A} \) and \( Q_{2B} \).

An alternative circuit is shown in Fig. 4.11(b), where the diode connection on transistors \( Q_{2A} \) and \( Q_{2B} \) have been reversed. Now there is a diode connection on either side of this circuit, and we might expect that the effect of finite \( \beta \) would be reduced. We begin this analysis in the same manner as for the Fig. 4.11(a) circuit, by observing that the emitter current of \( Q_{1B} \) is \( I_{OUT}(1 + 1/\beta) \), and the emitter current of \( Q_{1A} \) is \( (I_{REF} - I_{OUT}/\beta) \) - these expressions are identical for the Fig. 4.11(a) circuit. By observing the action of the current mirror realized by \( Q_{2A} \) and \( Q_{2B} \), we write the following KCL equation at the emitter of \( Q_{1B} \):

\[
I_{OUT} \left( 1 + \frac{1}{\beta} \right) = \left( I_{REF} - \frac{I_{OUT}}{\beta} \right) \left( 1 + \frac{2}{\beta} \right)
\]
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Solving the above equation gives:

\[
\frac{I_{\text{OUT}}}{I_{\text{REF}}} = \frac{1 + \frac{2}{\beta}}{1 + \frac{2}{\beta} + \frac{2}{\beta^2}}
\]

\[
\rightarrow \frac{\Delta I}{I_{\text{REF}}} = \frac{\frac{2}{\beta^2}}{1 + \frac{2}{\beta} + \frac{2}{\beta^2}} 
\approx -\frac{2}{\beta^2}
\]

This circuit indeed does realize a current mirror with the error reduced by a factor of \(2/\beta\) compared to the conventional cascode.

Notice that the Fig. 4.11(b) circuit has another important distinction from the Fig. 4.11(a) cascode configuration: The small-signal resistance from the \(Q_{1B}\) emitter to ground is now \(r_{e2}\) - a relatively small resistance. The high output resistance of this circuit comes from the fact that the small-signal voltage that appears across \(Q_{2B}\) is multiplied by transconductance \(g_mQ\); this small-signal current is then mirrored into the equivalent resistance looking into the emitter of \(Q_{1A}\). A portion of the resulting negative small-signal voltage is then applied to the base of \(Q_{1B}\). Thus the \(v_r\) of \(Q_{1B}\) becomes negative as in a standard cascode, but in this case it is because both the emitter voltage increases and the base voltage decreases. This general concept is illustrated in Fig. 4.11(c). The small-signal emitter current of \(Q_{1B}\) is conducted into \(R_x\). The resulting voltage across \(R_x\) is amplified and inverted, and then applied to the \(Q_{1B}\) base voltage. This causes a large negative small-signal voltage between the base and emitter of \(Q_{1B}\), which makes the output resistance very large. This structure is known as a “regulated cascode” and is common in MOSFET current sources as well. The details of the analysis of the Fig. 4.11(b) circuit have been left as a homework exercise.

4.5 Advanced Current Sources: Supply, Temperature Independence

4.5.1 Power Supply Dependence of Current Sources

For the current mirrors described so far in this chapter, the reference current \(I_{\text{REF}}\) is developed by applying a well-defined voltage – the supply voltage less a smaller value (usually a \(V_{BE}\) or \(V_{GS}\) for the simplest current mirror structure) – across a resistor. It is often useful to accurately characterize the
sensitivity of a reference current to the supply voltage. This is because in practice the supply voltage can vary for a variety of reasons. The following is an example of how this calculation is performed on the Fig. 4.3(d) reference and output currents.

We begin by writing the expression for $I_{\text{REF}}$ in terms of the relevant voltages:

$$I_{\text{REF}} = \frac{1}{R_{\text{REF}}} \cdot (V_{\text{CC}} - V_{\text{BE}}) \quad (4.36)$$

We now take the derivative of the above equation with respect to $V_{\text{CC}}$ to see how a small change in the supply voltage will perturb $I_{\text{REF}}$:

$$\frac{dI_{\text{REF}}}{dV_{\text{CC}}} = \frac{1}{R_{\text{REF}}} \cdot \left(1 - \frac{dV_{\text{BE}}}{dV_{\text{CC}}} \right) \quad (4.37)$$

In order to find an expression for $dV_{\text{BE}}/dV_{\text{CC}}$ in (4.37), we can write the following expression:

$$V_{\text{BE}} = V_T \cdot \ln \frac{I_{\text{REF}}}{I_{\text{ES}}} \quad (4.38)$$

Using the chain rule, we take the derivative of the above equation with respect to $V_{\text{CC}}$:

$$\frac{dV_{\text{BE}}}{dV_{\text{CC}}} = \frac{dV_{\text{BE}}}{I_{\text{REF}}} \cdot \frac{dI_{\text{REF}}}{dV_{\text{CC}}}$$

$$= \frac{V_T}{I_{\text{REF}}} \cdot \frac{dI_{\text{REF}}}{dV_{\text{CC}}} \quad (4.39)$$

Substituting (4.39) in (4.37), we have:

$$\frac{dI_{\text{REF}}}{dV_{\text{CC}}} = \frac{1}{R_{\text{REF}}} \cdot \left(1 - \frac{V_T}{I_{\text{REF}}} \cdot \frac{dI_{\text{REF}}}{dV_{\text{CC}}} \right) \quad (4.40)$$

Notice that this is an implicit equation in $dI_{\text{REF}}/dV_{\text{CC}}$ since this derivative appears on both sides of the equation. This presence of the derivative on the right-hand side of the equation can be interpreted as follows: As $V_{\text{CC}}$ increases, $I_{\text{REF}}$ increases, thereby requiring a small increase in the transistor $V_{\text{BE}}$, which results in a slight decrease in $I_{\text{REF}}$. (As we'll see shortly, this effect is normally quite small.) Solving (4.40) gives:

$$\frac{dI_{\text{REF}}}{dV_{\text{CC}}} = \frac{1}{R_{\text{REF}}} \cdot \frac{1}{1 + \frac{V_T}{I_{\text{REF}}} \cdot \frac{dI_{\text{REF}}}{dV_{\text{CC}}}} \quad (4.41)$$
4.5. ADVANCED CURRENT SOURCES: SUPPLY, TEMPERATURE INDEPENDENCE

It is usually convenient and more meaningful to express the sensitivity in normalized units – that is, we define the following expression for the sensitivity of \( I_{\text{REF}} \) with respect to \( V_{\text{CC}} \):

\[
S_{V_{\text{CC}}}^{I_{\text{REF}}} = \frac{V_{\text{CC}}}{I_{\text{REF}}} \cdot \frac{dI_{\text{REF}}}{dV_{\text{CC}}} = \frac{dI_{\text{REF}}/I_{\text{REF}}}{dV_{\text{CC}}/V_{\text{CC}}}
\]

This expression gives the ratio of the incremental change in \( I_{\text{REF}} \) to the given incremental change in \( V_{\text{CC}} \). Applying this to (4.41) we have:

\[
S_{I_{\text{REF}}}^{V_{\text{CC}}} = \frac{V_{\text{CC}}}{I_{\text{REF}}} \cdot \frac{1}{1 + \frac{R_{\text{REF}}}{I_{\text{REF}}R_{\text{REF}}}} = \frac{V_{\text{CC}}}{I_{\text{REF}}R_{\text{REF}}} \cdot \frac{1}{1 + \frac{V_{T}}{I_{\text{REF}}R_{\text{REF}}}} \tag{4.42}
\]

Replacing \( I_{\text{REF}}R_{\text{REF}} \) with \( V_{\text{CC}} - V_{\text{BE}} \), we can rewrite (4.42) as:

\[
S_{I_{\text{REF}}}^{V_{\text{CC}}} = \frac{V_{\text{CC}}}{V_{\text{CC}} - V_{\text{BE}}} \cdot \frac{1}{1 + \frac{V_{T}}{V_{\text{CC}} - V_{\text{BE}}}} \tag{4.43}
\]

If we assume that \( V_{\text{CC}} - V_{\text{BE}} \gg V_{T} \), then (4.43) can be approximated as:

\[
S_{I_{\text{REF}}}^{V_{\text{CC}}} \approx \frac{V_{\text{CC}}}{V_{\text{CC}} - V_{\text{BE}}} \tag{4.44}
\]

(Note that taking this approximation amounts to ignoring the variation of \( V_{\text{BE}} \) with \( V_{\text{CC}} \) compared to the variation in \( I_{\text{REF}}R_{\text{REF}} \).

The normalized expression in (4.44) gives the percentage change in \( I_{\text{REF}} \) as the result of a 1% change in \( V_{\text{CC}} \). It is clear from this expression that the sensitivity is slightly larger than 1 – that is, any relative deviation in \( V_{\text{CC}} \) will give nearly the same relative deviation in \( I_{\text{REF}} \). This is to be expected, since a change in \( V_{\text{CC}} \) directly changes the current in \( R_{\text{REF}} \).

Since the current mirror sets \( I_{\text{REF}} = I_{\text{OUT}} \), then \( S_{I_{\text{OUT}}}^{V_{\text{CC}}} = S_{I_{\text{REF}}}^{V_{\text{CC}}} \). This behavior is not desirable in the presence of supply voltage variations. The supply voltage must be provided externally. A number of factors can cause variations in this voltage on the chip: First, changes in temperature can cause the circuit generating the voltage to vary. Second, once the voltage is applied to the integrated circuit, internal IR drops can reduce the voltage that is actually applied to the current mirror itself. These IR drops, which depend on the resistance of the metal lines, can themselves change over processing and temperature. Thus it is highly desirable to generate a reference current that is not very sensitive to the supply voltage – that is, one with a sensitivity that is much lower than unity.
4.5.2 Biasing Based on Other Voltages

To realize a current source that is less dependent on the supply voltage, we might first think about voltages other than the supply that might be available on the chip; two are already familiar:

- $V_{BE}$ of a BJT with a constant current
- $V_t$ of a MOSFET

There are two other voltages that can be generated that will also prove to be useful shortly:

- $\Delta V_{BE}$: The difference in $V_{BE}$s of two BJTs or diodes with different current densities.
- $V_{BG}$: The \textit{bandgap voltage} of silicon.

$V_{BE}$ Reference

Consider the circuit shown in Fig. 4.12(a). Like the simple current source we have already analyzed, it consists of two branches, $I_{REF}$ and $I_{OUT}$. However, unlike the previous circuit, it does not contain a current mirror. The function of the $I_{REF}$ branch is to create a voltage across the two diode-connected transistors $Q_1$ and $Q_2$. The voltage $V_{BE1} + V_{BE2}$ across these transistors is applied to the base of $Q_3$ and thus the voltage across resistor
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$R_E$ is $V_{BE1} + V_{BE2} - V_{BE3}$. Thus, ignoring base currents, we can write for this circuit:

$$I_{OUT} = \frac{V_{BE1} + V_{BE2} - V_{BE3}}{R_E}$$  \hspace{1cm} (4.45)

If we first assume that each $V_{BE}$ is roughly the same (often a reasonable assumption for BJTs), then the above equation simplifies to:

$$I_{OUT} \approx \frac{V_{BE}}{R_E}$$  \hspace{1cm} (4.46)

It is now apparent why this circuit is known as a “$V_{BE}$ reference” – the output current is proportional to $V_{BE}$, and the desired current value can be realized simply by setting the appropriate $R_E$. Note that, to a first order, $I_{OUT}$ is no longer directly dependent on $I_{REF}$. While $I_{REF}$ is still nearly proportional to $V_{CC}$, $I_{OUT}$ is not. Thus we would expect this circuit to exhibit substantially lower supply sensitivity as compared to the simple current mirror.

To analyze more accurately the sensitivity of the Fig. 4.12(a) circuit, we can write the following equations for the two currents; we now take into account the exact values of each transistors $V_{BE}$, but we are still ignoring the transistor base currents. Since $I_{REF}$ is conducted through both $Q_1$ and $Q_2$, we will define $V_{BE1,2} \equiv V_{BE1} = V_{BE2}$.

$$I_{REF} = \frac{1}{R_{REF}} [V_{CC} - 2V_{BE1,2}]$$  \hspace{1cm} (4.47)

$$I_{OUT} = \frac{1}{R_E} [2V_{BE1,2} - V_{BE3}]$$  \hspace{1cm} (4.48)

Taking the derivative of (4.47) and recognizing that for a BJT biased in the forward-active region $\frac{dV_{BE}}{dC} = \frac{V_T}{I_C}$, we have:

$$\frac{dI_{REF}}{dV_{CC}} = \frac{1}{R_{REF}} \cdot \left[ 1 - \frac{2V_T}{I_{REF}} \cdot \frac{dI_{REF}}{dV_{CC}} \right]$$  \hspace{1cm} (4.49)

Solving this expression in a way similar to that in (4.40), we have:

$$\frac{dI_{REF}}{dV_{CC}} = \frac{1}{1 + \frac{2V_T}{I_{REF}^2}}$$  \hspace{1cm} (4.50)

As expected, the supply sensitivity of $I_{REF}$ for this circuit is similar to that of the Fig. 4.3(d) current mirror. We now find the supply sensitivity of $I_{OUT}$ by taking the derivative of (4.48), which gives:

$$\frac{dI_{OUT}}{dV_{CC}} = \frac{1}{R_E} \left[ 2 \frac{V_T}{I_{REF}} \cdot \frac{dI_{REF}}{dV_{CC}} - \frac{V_T}{I_{OUT}} \cdot \frac{dI_{OUT}}{dV_{CC}} \right]$$  \hspace{1cm} (4.51)
Plugging in the expression for \( dI_{REF}/dV_{CC} \) found in (4.50) into (4.51) and solving for \( dI_{OUT}/dV_{CC} \), we have:

\[
\frac{dI_{OUT}}{dV_{CC}} = \frac{2V_T}{I_{REF}R_{REF}} \cdot \frac{1}{1 + \frac{2V_T}{I_{REF}R_{REF}}} \tag{4.52}
\]

Thus the sensitivity is given by:

\[
S_{I_{OUT}}^{V_{CC}} = \frac{V_{CC}}{I_{REF}R_{REF}} \cdot \frac{2V_T}{I_{OUT}R_E} \cdot \frac{1}{1 + \frac{2V_T}{I_{REF}R_{REF}}} \tag{4.53}
\]

Substituting \( I_{OUT}R_E = V_{BE} \) and \( I_{REF}R_{REF} = V_{CC} - 2V_{BE} \) into the above equation and assuming \( I_{REF}R_{REF} \gg V_T \), we have:

\[
S_{I_{OUT}}^{V_{CC}} \approx \frac{V_{CC}}{V_{CC} - 2V_{BE1,2}} \cdot \frac{2V_T}{V_{BE3}} \tag{4.54}
\]

\[
\approx \frac{2V_T}{V_{BE3}} \cdot \frac{1}{1 - \frac{V_{BE1,2}}{V_{CC}}} \tag{4.55}
\]

If we plug in typical values of \( V_{CC} = 3.3 \) V, \( V_T = 0.026 \) V and \( V_{BE3} = 0.7 \) V, this gives a sensitivity of about 0.13 – almost an order of magnitude improvement over the simple current mirror!

The Fig. 4.12(a) has a rather simple structure; in particular, the reference branch is separate from the output branch. In other words, as \( V_{CC} \) increases, \( I_{REF} \) will increase, thereby increasing (by a much smaller increment) the voltages across diode-connected transistors \( Q_1 \) and \( Q_2 \). As a result, the voltage at the base of \( Q_3 \) also increases, which finally results in an increase in \( I_{OUT} \). The much smaller sensitivity that we have just calculated is due to the fact that \( I_{REF} \) increases almost linearly with \( V_{CC} \) as expressed in (4.47), while \( I_{OUT} \) increases only logarithmically with \( I_{REF} \) as expressed in (4.48).

We can improve the operation of this circuit by making a slight change in its topology as shown in Fig. 4.12(b). By disconnecting the base terminal of \( Q_1 \) from its own collector terminal and instead connecting it to the base of \( Q_3 \), \( I_{OUT} \) now depends only on \( V_{BE1} \), rather than the \( V_{BE} \) of all transistors as expressed in (4.45) for the Fig. 4.12(a) circuit. Since for the Fig. 4.12(b) circuit \( I_{OUT} \) varies with only one \( V_{BE} \) rather than two, we would expect its sensitivity to be roughly half that of the Fig. 4.12(a) circuit. We’ll analyze this in more detail shortly; first we will verify that the Fig. 4.12(b) circuit operates in the same way as that of the Fig 4.12(b) circuit. Assuming that all transistors are turned on, we see that the voltage at the base of \( Q_1 \) is
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$V_{BE1}$, which means that the voltage at the base of $Q_3$ must be $V_{BE1} + V_{BE2}$. Thus we can write:

$$I_{REF} = \frac{1}{R_{REF}} (V_{CC} - V_{BE3} - V_{BE12}) \quad (4.56)$$

$$I_{OUT} = \frac{V_{BE12}}{R_E} \quad (4.57)$$

Although these equations are different from (4.47) and (4.48), they give nearly identical results for the dc biasing.

Performing the same analysis as for the Fig. 4.12(a) circuit and making the same assumptions about the dc voltages (the actual calculations have been left as a homework exercise), we find that the supply sensitivity for the Fig. 4.12(b) circuit is given by:

$$S_{VCC}^{OUT} \approx \frac{V_{CC}}{I_{REF}R_{REF}} \cdot \frac{V_T}{I_{OUT}R_E} \quad (4.58)$$

$$= \frac{V_T}{1 - \frac{1}{2} \frac{V_{BE12}}{V_{CC}}} \quad (4.59)$$

That is, the sensitivity of the Fig. 4.12(b) circuit is just about half that of the Fig. 4.12(a) circuit.

Finally, we observe that transistor $Q_2$ in the Fig. 4.12(b) circuit has no critical function; its $V_{BE}$ does not enter into the (4.56) and (4.57) equations. In fact, if we simply remove this transistor and short the two remaining nodes together, as shown in the Fig. 4.12(c) circuit, the behavior is essentially identical as that of Fig. 4.12(b) except that the expression for $I_{REF}R_{REF}$ is larger by one additional $V_{BE}$ drop.

### 4.5.3 $V_t$ Current Reference

A current reference very similar to the $V_{BE}$ reference in Fig. 4.12(c) is shown in Fig. 4.13(a). We can write the following expression for this circuit:

$$I_{REF} = \frac{1}{R_{REF}} (V_{DD} - V_{GS3} - V_{GS1}) \quad (4.60)$$

$$I_{OUT} = \frac{V_{GS1}}{R_S} \quad (4.61)$$

Unlike the BJT case, we cannot automatically assume that $V_{GS1}$ remains nearly constant over even moderate changes in $I_{REF}$. In particular, we can
write the dependence as follows:

\[ V_{GS1} = V_t + \sqrt{\frac{2I_{REF}}{k'(W/L)}} \]  \hspace{1cm} (4.62)

From the above equation we see that if we make \( W/L \) large, the part of the expression for \( V_{GS1} \) will dependent on \( I_{REF} \) will be small, thus making \( V_{GS1} \) very close to \( V_t \), a constant. It is for this reason that this circuit, with \( W/L \) made sufficiently large, is known as a “\( V_t \) reference.”

### 4.5.4 Bootstrapping

In the two reference circuits presented in the previous section, the operation has been to first generate a reference current \( I_{REF} \), which then generates a voltage (\( V_{BE} \) or \( V_t \)), from which we generate the output current \( I_{OUT} \) that is proportional to the voltage. The decreased supply sensitivity stems from the fact that the voltage has much lower sensitivity to \( V_{DD} \) than \( I_{REF} \). These circuits were shown to give about two orders of magnitude lower sensitivity than the simple current mirror. This is a significant improvement, however there may be applications where even more precision is required. In thinking about how we might improve the sensitivity even more, we observe again that in the Fig. 4.12(c) and Fig. 4.13 circuits there are two currents generated: \( I_{REF} \) is a nearly linear function of the supply voltage, while \( I_{OUT} \) is a much weaker function of the supply voltage. How might we make \( I_{REF} \) less
sensitive to the supply? One way would be to instead set $I_{REF} = I_{OUT}$ by using a standard current mirror. Such a circuit is shown in Fig. 4.14(a), where $I_{REF}$ is now set to be equal to $I_{OUT}$ by the action of the pnp current mirror.

Since there is no longer a resistive coupling to $I_{REF}$ directly from $V_{DD}$, we would expect the sensitivity of this circuit to be lower. The supply sensitivity of this circuit can be estimated by starting with (4.58) and recognizing that $R_{REF}$ in Fig. 4.12(c) is replaced in the Fig. 4.14(b) bootstrapped version by $r_{o1}$, the output resistance of pnp transistor $Q_{1B}$. Making this substitution, we have:

$$\frac{V_{CC}}{I_{OUT}} \cdot \frac{dI_{OUT}}{dV_{CC}} \approx \frac{V_{CC}}{I_{REF} \cdot r_{o1}} \cdot \frac{V_{T}}{I_{OUT} R_{E}}$$

(4.63)

$$= \frac{V_{CC}}{V_{A(pnp)}} \cdot \frac{V_{T}}{V_{BE2}}$$

(4.64)

Comparing the results in (4.58) and (4.64), we can see that the improvement by using the bootstrapped version is a factor of $V_{A(pnp)} / V_{CC} - V_{BE}$, which is typically on the order of about 30. Thus the bootstrapped version improves the sensitivity by more than another order of magnitude. (An exact analysis of this circuit’s sensitivity is left as a homework exercise.)