Motivation for CDR: Deserializer (1)

If input data were accompanied by a well-synchronized clock, deserialization could be done directly.
Motivation for CDR (2)

- Providing two high-speed channels (for data & clock) is expensive.
- Alignment between data & clock signals can vary due to different channel characteristics for the different frequency components. Hence retiming would still be necessary.

PLLs naturally provide synchronization between external and internal timing sources. A CDR is often implemented as a PLL loop with a special type of PD...
Return-to-Zero vs. Non-Return-to-Zero Formats

NRZ

RZ

RZ spectrum has energy at $1/T_b \implies$ conventional phase detector can be used.

NRZ spectrum has null at $1/T_b \implies$ ??
Phase Detection of RZ Signals

- Phase detection operates same as for clock signals for logic 1.
- $V_d$ exhibits 50% duty cycle for logic 0.
- $K_{pd}$ will be data dependent.
Phase Detection of NRZ Signals

Since data rate is half the clock rate, multiplying phase detection is ineffective.

- RZ signals can use same phase detector as clock signals
- RZ data path circuitry requires bandwidth that is double that of NRZ.
- Different type of phase detection required for NRZ signals.
Idea: Mix NRZ data with delayed version of itself instead of with the clock.

Example: 1010 data pattern (differential signaling)
Operation of D Flip-Flops (DFFs)

CMOS transmission gate:

latch:

DFF:

Ideal waveforms:

Symbol:

No bubble ⇒ Q changes following rising edge of CK
DFF Setup & Hold Time

At CK rising edge, the master latches and the slave drives.

When a data transition occurs within the setup & hold region, metastability occurs.
DFF Clock-to-Q Delay

$t_{ck-q}$ is determined by delays of transmission gate and inverter.
Realization of Data/Data Mixing:

Delay between $D_{in}$ to $Q$ is related to phase between $D_{in}$ & $RCK$
Define zero phase difference as a data transition coinciding with RCK falling edge; i.e., RCK rising edge is in center of data eye.

\[ \Delta \phi = 2\pi \cdot \frac{\Delta t}{T_b} - \frac{1}{2} \]

\[ \Delta t = T_b \left[ \frac{\Delta \phi}{2\pi} + \frac{1}{2} \right] \]
Phase detector characteristic also depends on transition density:

0101… pattern:

\[ V_P = V_{swing} \cdot \left( \frac{\Delta t}{T_b} - \frac{1}{2} \right) \]

0011… pattern:

\[ V_P = V_{swing} \cdot \left( \frac{\Delta t}{2T_b} - \frac{1}{2} \right) \]

In general,

\[ V_P = V_{swing} \cdot \left( \alpha \frac{\Delta t}{T_b} - \frac{1}{2} \right) \]

where \( \alpha \equiv \) average transition density
Constructing CDR PD Characteristic

\[
\frac{\Delta t}{T_b} = \frac{\Delta \phi}{2\pi} + \frac{1}{2}
\]

\[
\frac{V_P}{V_{\text{swing}}} = \alpha \frac{\Delta t}{T_c} - \frac{1}{2}
\]

\[
\frac{\bar{V}_P}{V_{\text{swing}}} = \alpha \frac{2\pi}{\Delta \phi} + \frac{(\alpha - 1)}{2}
\]

slope: \( K_{pd} = \frac{\alpha}{2\pi} \)

intercept: \( \Delta \phi = 0 \Rightarrow \frac{\bar{V}_P}{V_{\text{swing}}} = \frac{\alpha - 1}{2} \)

Both slope and offset of phase-voltage characteristic vary with transition density!
To cancel phase offset:

\[ D \]

\[ R \]

\[ \text{Always 50\% duty cycle; average value is } (\alpha - 1) \cdot V_{\text{swing}} / 2 \]

\[ \frac{V_p - V_R}{V_{\text{swing}}} \]

\[ \alpha = 1 \]

\[ \alpha = 0.5 \]

\[ K_{pd} \text{ still varies with } \alpha, \text{ but offset variation cancelled.} \]

Transconductance Block
Due to inherent mixing operation, Hogge PD is not a good frequency detector. A frequency acquisition loop with a reference clock is usually needed:

Non-Idealities in Hogge Phase Detector:
A. Clock-to-Q Delay (1)

\[ D_{in} = D_{in} \oplus Q \]
\[ R = Q \oplus Q_{R} \]
Non-Idealities in Hogge Phase Detector:
A. Clock-to-Q Delay (2)

Result is an input-referred phase offset:

\[ \phi_{os} = 2\pi \frac{t_{ck-Q}}{T_b} \]
Non-Idealities in Hogge Phase Detector:
A. Clock-to-Q Delay (3)

Phase offset moves RCK away from center of data, making retiming less robust.
Non-Idealities in Hogge Phase Detector:

A. Clock-to-Q Delay (4)

Use a compensating delay:

\[ \Delta t \approx t_{CK-Q} \]

\[ D \]

\[ D_{\Delta t} \]

\[ D_{in} \]

\[ RCK \]

\[ Q \]

\[ Q_R \]

\[ P \]

\[ R \]

\[ t_{ck-Q} \]
Non-Idealities in Hogge Phase Detector:
B. Delay Between $P$ & $R$ (1)

$D_{in}$

$RCK$

$P$ and $R$ are offset by 1/2 clock period

$Q$

$Q_R$

$P$

$R$
Non-Idealities in Hogge Phase Detector:
B. Delay Between $P$ & $R$ (2)

Average value of $V_{control}$ is well-controlled, but resulting ripple causes high-frequency jitter.
Non-Idealities in Hogge Phase Detector:
B. Delay Between $P$ & $R$ (3)

Idea: Based on $R$ output, create compensating pulses:

Standard Hogge/charge pump operation for single input pulse:

$D_{in}$, $RCK$, $Q$, $Q_R$, $P$ (up), $R$ (dn), $V_{control}$
Non-Idealities in Hogge Phase Detector:

B. Delay Between $P$ & $R$ (4)

Cancels out effect of next pulse
Other Nonidealities of Hogge PD (1)
Other Nonidealities of Hogge PD (2)

Effect of Transition Density:

![Graph showing the effect of transition density on different patterns: 1010 pattern, 1100 pattern, and PRBS pattern.](image)
Other Nonidealities of Hogge PD (3)

Effect of DFF bandwidth limitation:
Other Nonidealities of Hogge PD (4)

Effect of XOR bandwidth limitation:

Since the PD output signals are averaged, XOR bandwidth limitation has negligible effect.
Other Nonidealities of Hogge PD (5)

Effect of XOR Asymmetry:

![Graph showing PRBS data with delayed data connected to the slow and fast ports.](image)
Binary Phase Detectors

Idea: Directly observe phase alignment between clock & data

Clock falling edge early: Decrease $V_{control}$
Clock falling edge centered: No change to $V_{control}$
Clock falling edge late: Increase $V_{control}$

Ideal binary phase-voltage characteristic:

Also known as “bang-bang” phase detector
**D Flip-Flop as Phase Detector**

<table>
<thead>
<tr>
<th>Early clock:</th>
<th>Late clock:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data transitions align with clock low</td>
<td>Data transitions align with clock high</td>
</tr>
</tbody>
</table>

Realization using double-clocked DFF; note that RCK/Din connections are reversed:

Top (bottom) DFF detects on Din rising (falling) edge; DFF selected by opposite Din edge to avoid false transitions due to clock-q delay.
What happens if $\Delta \phi = 0$?

- If transition at $D$ input occurs within setup/hold time, *metastable operation* results.
- $Q$ output can “hang” for an arbitrarily long time if zero crossings of $D$ & $CK$ occur sufficiently close together.
- Metastable operation is normally avoided in digital circuit operation(!)
Dog Dish Analogy

A dog placed equidistant between two dog dishes will starve (in theory).
Non-Idealities in Binary DFF Phase Detector

1. Metastable operation difficult to characterize & simulate, varies widely over processing/temperature variations. $K_{pd}$ (and therefore jitter transfer function parameters) are difficult to analyze. **Exact value of $K_{pd}$ depends on metastable behavior and varies with input jitter.**

2. Large-amplitude pattern-dependent variation is present in phase detector output while locked.

3. During long runs phase detector output remains latched, resulting in VCO frequency changing continuously:

\[
\begin{align*}
D_{in} & \quad RCK & \quad V_P & \quad f_{vco} \\
\quad & \quad & \quad & \quad
\end{align*}
\]
Idea: Change VCO frequency for only one clock period

Circuit realization should sample data with clock (instead of clock with data) while maintaining bang-bang operation.
Alexander Phase Detector

- **D\textsubscript{in}**
- **RCK**
- **Q\_1**
- **Q\_2**
- **Q\_3**
- **Q\_4**
- **UP**
- **DN**

**RCK early**
- \(Q\_1\) leads \(Q\_3\)
- \(Q\_2/\overline{Q\_4}\) in phase

**RCK late**
- \(Q\_3\) leads \(Q\_1\)
- \(\overline{Q\_1}/Q\_4\) in phase
Simulation Results: Alexander PD

DFF outputs

VCO control voltage
Simulation Comparison: Linear vs. Binary

Linear PD
- very small freq. acquisition range
- low steady-state jitter

Binary PD
- high freq. acquisition range
- high steady-state jitter
Half-Rate CDRs

To relax speed requirements for a given fabrication technology, a *half-rate* clock signal can be recovered:

- $D_{in}$: input data
- $RCK$: full-rate recovered clock
- $RCK2$: half-rate recovered clock

- Can be used in applications (e.g., deserializer) where full-rate clock is not required.
- Duty-cycle distortion will degrade bit-error ratio & jitter tolerance compared to full-rate versions.
Idea 1: Input data can be immediately demultiplexed with half-rate clock

\[ \text{Din} \quad RCK2 \quad \text{DA} \]

\[ \text{Din} \quad \text{DA} \quad \text{DB} \quad \text{synchronized with clock transitions} \]

\[ \text{RCK2} \]

\[ \text{Din} \quad \text{D0} \quad \text{D1} \quad \text{D2} \quad \text{D3} \quad \text{D4} \]

\[ \text{DA} \quad \text{D0} \quad \text{D2} \quad \text{D4} \]

\[ \text{DB} \quad \text{D1} \quad \text{D3} \]
Splitting D flip-flops into individual latches:

These pulse widths contain phase information.
Complete Linear Half-Rate PD

Idea 2: Observe timing between $D_{in}$, $RCK$ and quadrature $RCKQ$

$D_{in}$

$RCK$

$RCKQ$

$S_0$, $S_2$ sampled with RCK transitions

$S_1$ sampled with RCKQ transitions

Phase logic:

$(S_0 \oplus S_1 = 0)$ and $(S_1 \oplus S_2 = 1)$ \implies$ clock early

$(S_0 \oplus S_1 = 1)$ and $(S_1 \oplus S_2 = 0)$ \implies$ clock late

$(S_0 \oplus S_1 = 0)$ and $(S_1 \oplus S_2 = 0)$ \implies$ no transition
DLL-Based CDRs

- CMU JBW can be optimized to minimize $f_{ck}$ jitter.
- No VCO inside CDR loop; less jitter generation.
- Can be arranged to have faster lock time.

![Diagram of DLL-Based CDRs](image)
Fast-Lock CDR for Burst-Mode Operation

Gated ring oscillator:

```
EN
EN high: 7-stage ring oscillator
EN low: no oscillation
```

CDR based on 2 gated ring oscillators:

Each ring oscillation waveform is forced to sync with one of the $D_{in}$ phases.