

Lossless, Passive Soft Switching Methods for Inverters and Amplifiers

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Abstract— This paper proposes new lossless passive soft switching methods for inverters developed from a synthesis procedure applicable to all PWM converters. The lossless passive soft-switching converter properties and synthesis procedure are described and extended here for inverters. Promising half-bridge and full-bridge soft-switching inverter examples are shown from the synthesis results. The voltage stress across the main switches can be easily maintained below 125% of V_{bus} . No transformers are used for energy recovery, eliminating their associated diode stress and leakage inductance problems. The soft turn-on full bridge contains only six components. The soft turn-on/turn-off half-bridge contains 12 components. The theoretical and experimental waveforms and analysis are given.

I. INTRODUCTION

Soft switching of PWM converters lowers switching losses allowing higher frequency operation and reduced electromagnetic interference (EMI). A higher switching frequency is advantageous because it enables size reduction of the magnetic components and increases the system bandwidth. Overall, these features increase the power density of the converter and improve dynamic performance. For PWM converters, soft switching can be broadly classified into two groups: passive soft switching and active soft switching. Passive soft switching is performed with passive components (i.e. L, C, R, and D) only, where active soft switching incorporates additional switches to achieve the result. Although active methods have received a lot of attention in recent years, passive soft switching has been given renewed notice as a better price/performance ratio alternative to their active counterparts [2,3]. Of the switching loss mechanisms (voltage and current overlap, diode reverse recovery, and the internal switch capacitance dissipated at turn-on), passive soft switching methods lower all the losses except the internal capacitance loss. Historically, these passive soft switching methods have been lossy, dissipating the recovered energy in resistors [4], however recently, many lossless and partially lossless techniques have been proposed [2,5-19].

The two necessary components that must be added to the circuit to achieve passive zero-current turn on and zero-voltage turn off are a small inductor and capacitor. The inductor provides zero-current turn on of the active switches and limits the reverse recovery of the diodes while the capacitor provides zero-voltage turn off of the active switches. Typically, an inductor and capacitor have been placed in series and parallel with each active switch. However,

many other locations are possible and may yield lower component count, simplify the circuit, and improve performance. Furthermore, the additional circuitry accompanying the capacitor and inductor are used to losslessly recover their energy to either the load or the input. There are many different proposed circuits to accomplish this. However, general topological and electrical properties can be derived that describe all possible circuits. By defining these topological and electrical properties, new passive soft switching circuits can be synthesized.

This paper proposes new lossless passive soft switching methods for inverters developed from a synthesis procedure applicable to all PWM converters. The lossless passive soft-switching properties and synthesis procedure derived in [1] is described and extended here for inverters in Section II. The synthesis procedure uses the properties to find all possible locations of the capacitor and inductor added to achieve soft switching. Then a set of circuit cells is constructed that can easily attach to the converter to recover the energy stored in these elements. Promising half-bridge and full-bridge soft-switching inverter examples are shown from the synthesis results. The voltage stress across the main switches can be easily maintained below 125% of V_{bus} . No transformers are used for energy recovery, eliminating their associated diode stress and leakage inductance problems. The soft turn-on full bridge contains only six components, half the components of a previously proposed soft turn-on circuit [17]. The soft turn-on/turn-off half-bridge contains 12 components, less than the lossless inverter proposed in [11]. The theoretical waveforms and analysis of the soft switching full-bridge are described in Sections III and IV and an experimental example of a soft turn-on full-bridge circuit is shown in Section V. A conclusion is given in Section VI.

II. PROPERTIES AND SYNTHESIS OF LOSSLESS PASSIVE SOFT SWITCHING INVERTERS

Properties of lossless soft switching converters were derived in [1] where complete descriptions and examples are given applicable to all PWM converters. The properties below are labeled identically with [1]. However, properties 1, and 8 from [1] are not shown here because they do not apply to inverters.

A. Definitions of Lossless Passive Soft-Switching PWM Converters.

The definitions below first list the components that describe the hard-switched PWM converter and then follow with

additional components that are added to allow lossless passive soft switching.

Hard switched PWM converter:

1. A set of DC voltage sources, $V_s = (V_{s_i}, i = 1, \dots, n_g)$
2. A single linear time invariant (LTI) resistor R .
3. A set of LTI inductors $L = (L_i, i = 1, \dots, n_l)$
4. A set of LTI capacitors $C = (C_i, i = 1, \dots, n_c)$
5. A set of active switches $S = (S_i, i = 1, \dots, n_s), n_s \geq 1$
6. A set of diodes $D = (D_i, i = 1, \dots, n_d)$

Passive elements for lossless soft switching:

1. A set of zero-current inductors $L_r = (L_{r_i}, i = 1, \dots, n_{l_r})$
 L_r provide zero-current turn on of active switches S .
2. A set of snubber inductors: $L_s = (L_{s_i}, i = 1, \dots, n_{l_s})$
3. A set of zero-voltage capacitors $C_r = (C_{r_i}, i = 1, \dots, n_{c_r})$
 C_r provide zero-voltage turn off of the active switches S
4. A set of snubber capacitors $C_s = (C_{s_i}, i = 1, \dots, n_{c_s})$
5. A set of snubber transformers $T_s = (T_{s_i}, i = 1, \dots, n_{t_s})$
6. A set of snubber diodes $D_s = (D_{s_i}, i = 1, \dots, n_{d_s})$

Voltage storage device (VSD): A VSD is a device or subcircuit that stores energy in the form of voltage. (e.g. capacitor, voltage supply, etc.)

Passive turn-on and turn-off snubbers: Sets of passive elements for soft switching that are added to the hard switched converter to limit the switch current and voltage during switch turn-on and turn-off intervals respectively.

B. Zero-Current Turn On of Active Switches:

This subsection describes the number and placement of the zero-current inductors (ZCL)s to allow zero-current turn on of all active switches.

Property 2. Zero-current Inductor placements for Multiple Active Switch PWM converters: From a hard switched converter topology, a sufficient conditions for the zero-current turn on of S_i is a zero-current inductor, L_{r_i} , is placed in all loops comprised of S_i , a nonempty subset of $(C \cup \{V_s\} \cup D)$ and a subset (maybe empty) of S (excluding S_i).

Property 3. Maximum number of zero-current inductors: To provide zero-current turn on of X active switches, a maximum number of X zero-current inductors is needed.

C. Energy Management for Zero-Current Inductors.

At each switching interval, additional circuitry must manage the energy in the ZCL for lossless operation and avoidance of large voltage spikes across the switches. There are many possible ways to control this energy transition, however all methods have similar topological and electrical properties.

Property 4. Management of inductor energy at either switch or diode turn off. To control the energy in L_{r_i} regardless of whether a active switch or diode turns off, L_{r_i} must be in a loop comprised of a nonempty subset of D_s and a VSD. The voltage polarity of VSD and the conduction direction of D_{s_i} must be such that the inductor energy will

transfer to and/or will charge from the VSD when a switch S_i turns off or a diode D_i recovers.

Reference [1] also derives a special case of property 4 where more than one management loop can be used. The VSD for property 4 may be a relatively “stiff” voltage device where the voltage does not change much from cycle to cycle. In the past, for inverter systems, this VSD is most often realized by a forward transformer coupling [9-17] as conceptually shown in Fig. 1a. One magnetic core can be saved by coupling directly to the ZCL inductor as mentioned in [4]. Although the ZCL energy is transferred directly to the bus voltage, it has several drawbacks. Using this transformer coupling in an inverter, the ideal voltage stress across the switch and diode are as follows:

$$V_{S_{i\max}} = V_{bus} \left(I + \frac{I}{n} \right) \quad V_{D_{s2\max}} = V_{bus} (I + n). \quad (1)$$

Equation (1) shows that to maintain a reasonable voltage stress across the main switch at turn off (i.e. $1.25V_{bus}$) the diode D_{s2} will have a voltage stress larger than $5V_{bus}$ when the switch is turned back on. This stress can be cut in half by increasing the circuit complexity [16,17]. Furthermore, the transformer’s leakage inductance can cause large voltage spikes when the switch is turned off. Therefore, all proposed circuits also use some additional voltage clamping action (either lossy or lossless) to control this leakage inductance energy.

An alternative realization of the VSD, which significantly reduces the circuit component count and diode voltage stress, is to use a relatively large capacitor as shown in Fig. 1b. The energy in the capacitor is accumulated from the management of the ZCL energy. It is recovered by inserting a second inductor and diode so that an L-C-D circuit is in parallel with the active switch. With this arrangement, when the active switch is conducting the capacitor is transferring the energy to the inductor as shown in Fig. 1b with the energy path. When the active switch turns off the inductor will transfer this energy to the input source. The voltage of the capacitor will adjust automatically so that at steady state the energy flowing into the capacitor equals the energy flowing out of the capacitor. In this case, the diodes have the same voltage stress as the main switch ($V_{bus} + V_{cs}$ for an inverter).

D. Zero-Voltage Turn Off of Active Switches

Capacitors may be used to turn off the main switches with zero voltage, called zero-voltage capacitors (ZVC)s. These can substantially reduce the turn-off loss of slower devices such as IGBTs.

Property 5. Zero-voltage capacitor Placement: For zero-voltage turn off of the active switch S_i , S_i must be in a loop with a nonempty subset C_r , a subset of $(C \cup \{V_s\} \cup C_s)$ and a nonempty subset of D_s . The diodes D_s in the loop must be in the direction to conduct the switch current when S_i turns off. The electrical requirement of this loop to ensure zero-

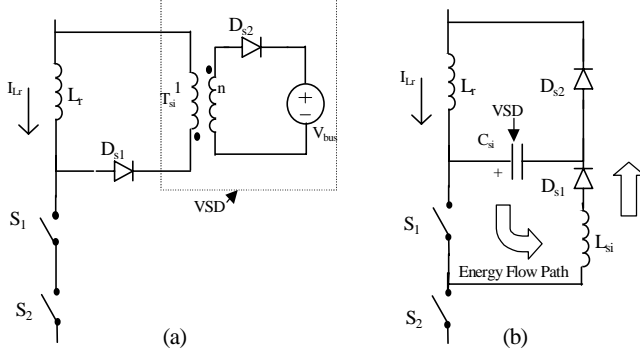


Fig. 1. Realization of VSD : (a) forward transformer coupling, (b) Large Capacitor C_s

voltage turn off is that when the switch S_i is opened and has zero parasitic capacitance, the voltage around the loop the moment after turn off must still be zero volts.

The snubber components (C_r , C_s , and D_s) that make up the loop satisfying property 5 are defined as the ZVC subcircuit. The other elements in the loop are part of the original hard switching topology.

Property 6: Zero-voltage capacitor subcircuit placement (Using terms in graph theory [24]) Every zero-voltage capacitor subcircuit represents a chord that creates a loop from the largest connected subgraph that contains switch S_i and a subset of $(C \cup \{V_s\})$. This subgraph is taken from the hard-switched converter topology unless a zero-current inductor has been inserted into the topology. Then the subgraph is taken from the hard-switched topology with the zero-current inductor L_r .

Property 7. Maximum number of zero-voltage capacitors: To provide zero-voltage turn off of X active switches, a maximum number of X zero-voltage capacitors C_r is needed.

E. Synthesis of Lossless Passive Soft Switching Inverters

The properties listed above allow the synthesis of lossless passive soft switching inverters. The synthesis process was described in [1] for DC/DC converters. It is extended here for voltage source inverters. Circuits realized with different locations of the ZCL, and the ZVC subcircuit, are described as the *basic* soft-switching topologies for a given hard-switched converter. All new and previously proposed lossless passive soft-switching PWM converters can be described by one of these *basic* soft-switching topologies. Often, several proposed circuits have used the same *basic* soft-switching topology. What makes the circuits different from one another is the passive elements added to recover and manage the energy trapped in the ZCL and ZVC. The number of additional components and their interconnections are virtually limitless. However, by using selected circuit cells presented in [1] with each *basic* soft-switching topology a lossless soft-switching inverter can be found. The steps in the synthesis procedure are as follows:

Step 1: Find the number and placement of the zero-current inductors. This involves a two step optimization process as follows:

1a. For each switch, find all loops satisfying property 2. Take the intersection of the elements of these loops to form a set of elements, called L_{si_loc} . This set determines where a single inductor can be inserted in series for zero-current turn on of that switch.

1b. With the n_s sets obtained from step 1a, take the element intersection. If this resulting set is non-empty, then only one ZCL is needed to provide zero-current turn on of all switches. Otherwise more than one inductor is needed and can be found by intersecting the sets with common elements. The resulting number of left over sets signifies the number of ZCLs. However, to find the optimum number of ZCLs, order and set intersection groupings do matter. For power electronic systems, the optimum number of inductors can usually be found by inspection.

1c. The sets from 1b determine the number of ZCLs and which elements the ZCL may be inserted on either side.

For example, applying step 1a to the full-bridge inverter results in L_{si_loc} sets for switches S_1, S_2, S_3, S_4 of $\{S_1, S_2, V_s\}$, $\{S_1, S_2, V_s\}$, $\{S_3, S_4, V_s\}$, $\{S_3, S_4, V_s\}$ respectively. The element intersection of the loop sets results in $\{V_s\}$. Only one inductor is needed to provide zero-current turn on of all switches and there are two placements of this inductor as shown in Table 1. Similarly, the half-bridge inverter requires only one inductor and its six locations are also shown in Table 1.

Step 2: For each inductor location obtained in step 1, identify the locations of the ZVC subcircuits.

2a. For each switch obtain the subgraph described by property 6. The ZVC subcircuit locations are the loops created by a single cord around the switch S_i .

2b. The number of ZVC subcircuit locations for each switch can be found by defining the number of elements in the subgraph on either side of the S_i as E_1 , and E_2 . The number of capacitor subcircuit locations for a given switch

TABLE 1
BASIC SOFT-SWITCHING TOPOLOGIES FOR HALF AND FULL-BRIDGE INVERTERS

	Half Bridge	Full Bridge
L_r locations		
C_r Locations	L1-3, L2-9, L3-9, L4-3, L5-4, L6-4	L1-4, L2-4
Total	32	8

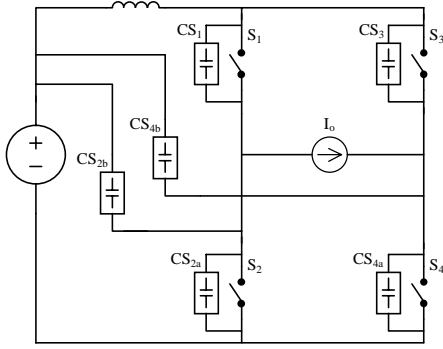


Fig. 2. Capacitor *subcircuit* locations for each switch

is as follows:

$$C_{Si_loc} = (1 + E_1)(1 + E_2) \quad (2)$$

2c. The total number of ZVC *subcircuit* combinations for a given inductor location is as follows:

$$C_{total_loc} = (C_{S1_loc})(C_{S2_loc}) \dots (C_{Sns_loc}) \quad (3)$$

Inserting one ZLC and ZVC *subcircuit* combination into a hard-switched topology make up one *basic* soft-switching topology. Together, all of the ZLC and ZVC *subcircuit* locations form all possible *basic* soft-switching topologies.

Table 1 shows the number of ZVC *subcircuit* locations for each inductor location. For example, with the ZCL in location L1 of the full-bridge, the possible number of ZVC *subcircuit* combinations is 4, listed as L1-4. These combinations can be seen in Fig. 2. Switches S_1 and S_3 each have one possible ZVC *subcircuit* location, CS1 and CS3 respectively. Switches S_2 and S_4 each have two locations, CS2a,b and CS4a,b. Using (3) obtains the four combinations of ZVC *subcircuits* that can be used when the inductor is in location L1. From table 1, using one ZCL, there are a total of 32 *basic* soft-switching topologies for the half-bridge inverter and 8 *basic* soft-switching topologies for the full-bridge inverter.

Step 3: For each *basic* soft-switching topology match one or more circuit cells to the ZCL and ZVC *subcircuit* locations to ensure the rest of the topological and electrical properties are satisfied.

Once a *basic* soft-switching topology is identified, circuit cells shown in [1] are used to provide the additional circuitry to control the inductor energy (property 4) and reset the ZVC (property 5). For hard switched converters with no passive switches (i.e. diodes), only circuit cells V, and VI from [1] need to be used and are displayed for convenience in Fig 3. For these two cells, C_s is a relatively large capacitor, which stores the inductor L_r and capacitor C_r energy from cycle to cycle. Elements C_r , C_s , and D_{s2} comprise the ZVC *subcircuit* for switch S. L_s is relatively large and transfers the energy in C_s to a subset of $(C \cup V_s)$. The cells in Fig 3 become just turn-on snubbers by removing the capacitor C_r

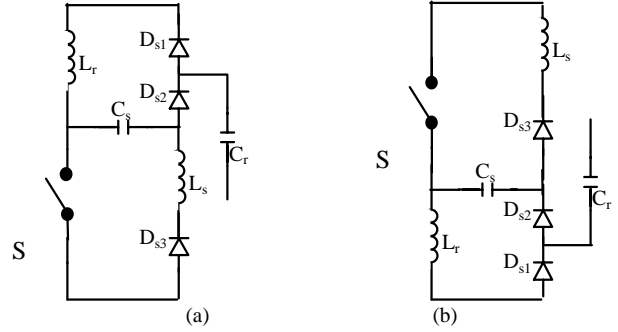


Fig. 3. Circuit cells using a capacitor VSD: (a)Cell V; (b)Cell VI.

and a diode D_{s1} . They also become just turn-off snubbers by not placing inductor L_r into a loop satisfying property 2.

An example of this synthesis procedure is shown in Fig. 4 for the full-bridge inverter with the ZCL placed in location L1. Fig. 4a shows the chosen starting *basic* soft-switching full-bridge topology. The circuit cell in Fig. 3a is then used to create the soft switching inverter shown in Fig. 4b. This inverter will provide soft turn on and turn off of all switches, and maintains lossless operation, but it has many components. Fortunately, many repeatable functions can be combined with one set of components, allowing the design to be simplified to Fig. 4c.

Figs. 5 and 6 shows several promising synthesis examples for a full-bridge and half-bridge inverter respectively. Each inverter has an extra winding on the L_{s1} core and the half bridge has two C_s capacitors that are used to maintain the C_s voltage below 25% of V_{bus} . Also shown in Figs. 5b and 6b are just the turn-on snubber versions of the circuits. To the authors' knowledge, these are the first proposed lossless passive snubber inverters that do not use transformer coupling to realize the VSD. Reference [10] shows a dissipative snubber that also does not use a transformer. Furthermore, for the half-bridge inverter, the voltage stress across all diodes is the same or less than the main switches ($V_{bus} + V_{cs}$).

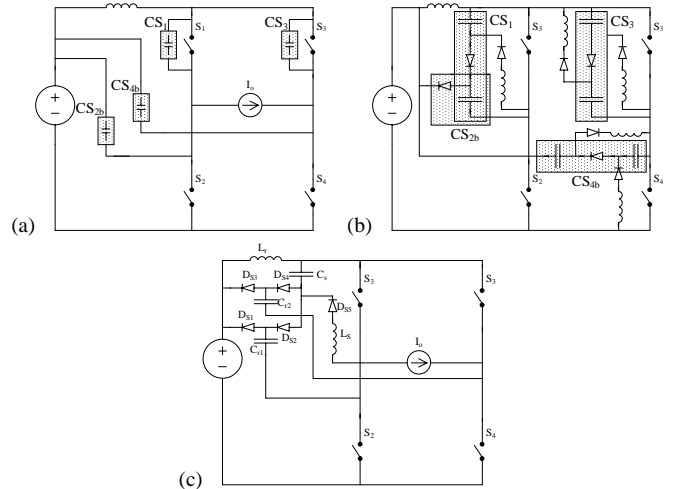


Fig. 4. Synthesis Example: (a) *basic* full-bridge topology; (b) Synthesis result; (c) Simplification

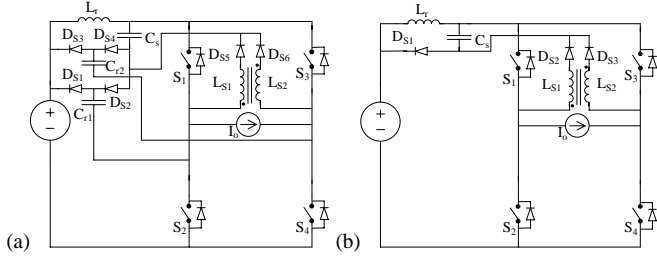


Fig. 5. Synthesis example full-bridge inverter: (a) Soft Turn-on/Turn-off; (b) Soft Turn-on;

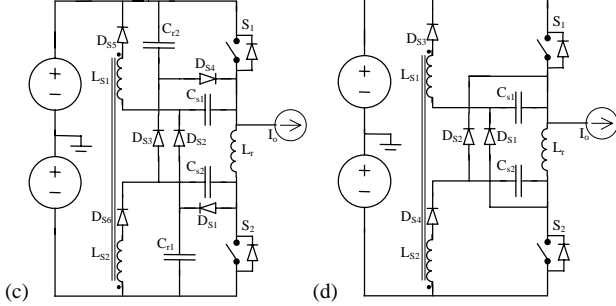


Fig. 6. Synthesis example half-bridge inverter: (a) Soft Turn-on/Turn-off; (b) Soft Turn-on;

This is the same for the full-bridge inverter when \$L_{s1}\$ and \$L_{s2}\$ are on separate cores. However, when using one core with the full-bridge inverter, the diodes in series with \$L_{s1}\$ and \$L_{s2}\$ (\$D_{s5}\$ and \$D_{s6}\$ in Fig. 5a) can reach \$(2V_{bus})\$. The full-bridge turn-on snubber contains only six components, The half-bridge turn-on/turn-off snubber contains 12 components.

III. OPERATION OF THE EXAMPLE LOSSLESS PASSIVE FULL-BRIDGE INVERTER

In this section, the operation of the example passive soft switching full-bridge inverter from Fig. 5a will be detailed. The operation of soft turn-on full bridge, Fig. 5b, and the half-bridge inverters shown in Figs. 6a and 6b are very similar and understanding should not be difficult once Fig. 5a is understood. As discussed in the last section, \$L_r\$ provides zero-current turn on of all switches and \$C_{r1}\$ and \$C_{r2}\$ provide zero-voltage turn off of switches \$S_1, S_2\$, and \$S_3, S_4\$ respectively. \$C_s\$ is the VSD that controls the ZCL and ZVC energy. The inductors \$L_{s1}\$ and \$L_{s2}\$ share the same magnetic core and are much larger than \$L_r\$. They are used to transfer the energy in \$C_s\$ to the bus supply. The operation will be described with the load current in the direction shown and the duty ratio, \$D\$, defined for the on time of switches \$S_1\$ and \$S_4\$. Operation for the opposite current direction has symmetrical characteristics.

Stage 1 (\$t_0-t_1\$): At time \$t_0\$, switches \$S_1\$ and \$S_4\$ are on and will be conducting the load current direction shown in Fig. 7a. The energy in \$C_s\$ is being partially transferred to \$L_{s1}\$ through switch \$S_1\$ with the current in \$L_{s1}\$ defined as:

$$i_{L_{s1}}(t) = \frac{V_{cs}}{L_{s1}}(t - t_0) \quad (4)$$

This current adds to the switch \$S1\$ current giving

$$i_{S1}(t) = I_o + \frac{V_{cs}}{L_{s1}}(t - t_0). \quad (5)$$

Stage 2 (\$t_1-t_2\$): At time \$t_1\$, \$S_1\$ and \$S_4\$ are turned off. The ZCL and load current, \$I_o\$, will charge and discharge \$C_{r1}\$ and \$C_{r2}\$ respectively as shown in Fig. 7b. \$C_{r1}\$ is charged through path \$C_s\$, \$D_{s2}\$ and \$C_{r2}\$ is discharged through \$D_{s3}\$. The \$dV/dt\$ of \$S1\$ and \$S4\$ are

$$\frac{dV_{S4}}{dt} = \frac{I_o}{C_{r2}} \quad \frac{dV_{S1}}{dt} = \frac{I_o + i_{L_{s1}}(t_1 - t_0)}{C_{r1}} \quad (6)$$

At time \$t_2\$, \$V_{Cr1} = V_{bus}\$ and \$V_{Cr2} = -V_{cs}\$ and the anti-parallel diodes of \$S_2\$ and \$S_3\$ start conducting. The off voltages of \$S_1\$ and \$S_4\$ is clamped to \$V_{bus} + V_{cs}\$.

*Stage 3 (\$t_2-t_4\$):*The load current and \$i_{L_{s1}}\$ path is shown in Fig. 7c where \$C_s\$ is being charged. The energy in \$L_{s1}\$ transfers to the input supply and \$C_s\$ controls the ZCL current until it reaches \$-I_o\$. At time \$t_3\$, \$i_{L_{s1}}\$ reaches zero amps. At this time, due to the coupling of \$L_{s1}\$ and \$L_{s2}\$, the voltage across \$D_{s6}\$ will drop from \$V_{bus} - V_{cs}\$ to zero and become forward biased. \$L_{s2}\$ then starts conducting. At time \$t_4\$, the current in \$L_r\$ reaches \$-I_o\$ and diodes \$D_{s1,2,3,4}\$ stop conducting. This completes the switch transition and the voltage across \$S_1\$ and \$S_4\$ returns to \$V_{bus}\$. If the time duration of stage 2 is much smaller than stage 3, then the switch transition time can be approximated as follows:

$$t_{stp} = t_4 - t_1 \approx \frac{2I_o L_r}{V_{cs}} \quad (7)$$

The energy transferred to the capacitor during this stage is

$$W_{C_{s_in1}} = \frac{1}{2} L_r (2I_o)^2 = 2L_r I_o^2. \quad (8)$$

Stage 4 (\$t_4-t_5\$): Fig. 7d shows the current conduction paths. The energy in \$C_s\$ is being partially transferred to \$L_{s2}\$ whose current during this stage is defined by

$$i_{L_{s2}}(t) = \frac{V_{cs}}{L_{s2}}(t - t_3). \quad (9)$$

This current subtracts from the load current though the anti-parallel diode of \$S3\$:

$$i_{S3}(t) = -I_o + \frac{V_{cs}}{L_{s2}}(t - t_3) \quad (10)$$

The approximate energy flowing out of the capacitor during this stage and stage 1 is found by assuming \$L_{s1}\$ and \$L_{s2}\$ are not coupled and are equal. The energy flowing out is the sum of

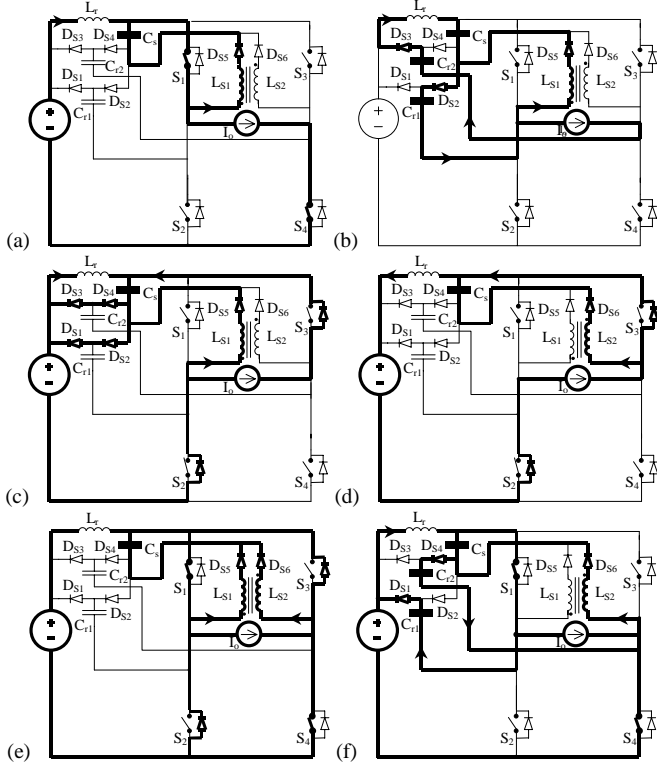


Fig. 7. Operating Stages of Soft Switching Full Bridge: (a) stage 1 (t_0 - t_1); (b) stage 2 (t_1 - t_2), (c) stage 3 (t_2 - t_4); (d) stage 4 (t_4 - t_5); (e) stage 5 (t_5 - t_7); (f) stage 6 (t_7 - t_0).

the energy in L_{s1} and L_{s2} at the end of stages 1 and 4. This energy can be found by replacing time with DT_s and $(1-D)T_s$ in (4) and (9) respectively. From this, the total energy taken from C_s can be found.

$$W_{C_{s_out}} \approx \frac{V_{cs}^2 T_s^2 ((1-D)^2 + D^2)}{2L_s} \quad (11)$$

Stage 5 (t_5 - t_7): At time t_5 , S1 and S4 are turned on with zero current. The current rise of S1 and S4 is

$$\frac{di_{S1,4}}{dt} = \frac{1}{2} \frac{V_{bus}}{L_r}, \quad (12)$$

Equation (12) assumes that the current in L_r splits equally between paths S_1 - S_2 and S_3 - S_4 as shown in Fig. 7e. The current L_r will ramp up until it reaches I_o at time t_6 and anti-parallel diodes of S_2 and S_3 will start to recover. In addition, during this stage both L_{s1} and L_{s2} are conducting. Because the cores are coupled, a voltage of $2V_{cs}$ is imposed across the leakage inductance, L_{Lkg} , of the L_{s1} - L_{s2} coupling. This will cause the current in switch S_1 to have an additional di/dt current of

$$\frac{di_{S1_extra}}{dt} = 2 \frac{V_{Cs}}{L_{Lkg}} \quad (13)$$

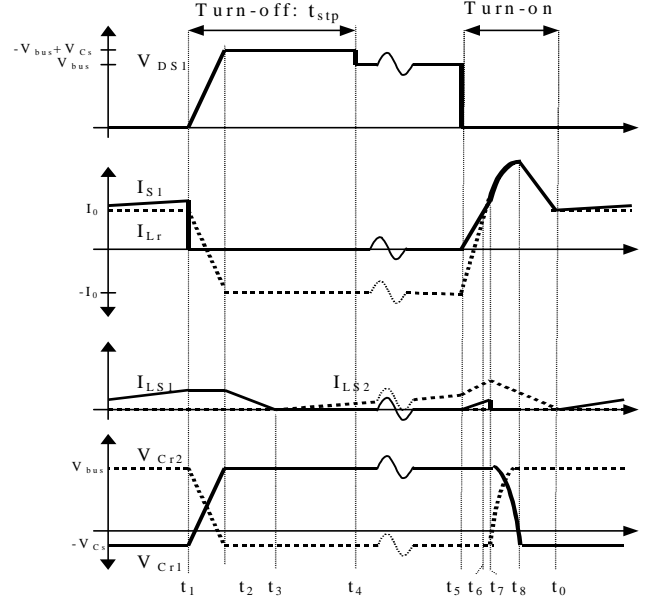


Fig. 8. Theoretical waveforms

By designing L_{s1} and L_{s2} coupling so that L_{Lkg} is much greater than L_r , and because V_{cs} is much smaller than V_{bus} it will have little effect and can be neglected. At time t_7 the diodes recover and the stage ends.

Stage 6 (t_7 - t_0): Once the anti-parallel diodes of S_2 and S_3 recover at t_7 , capacitors C_{r1} and C_{r2} will resonate with L_r until their voltages are reset to $-V_{cs}$ and V_{bus} respectively. The current in L_{s1} will stop and L_{s2} will transfer its energy to the output. C_{r1} resonates with L_r through D_{s1} and S_1 . C_{r2} resonates with L_r through C_s and D_{s4} . These two loops are effectively conducting in parallel providing an equivalent resonating frequency and impedance of:

$$\omega_n = \frac{1}{\sqrt{L_r(C_{r1}+C_{r2})}} \quad z_n = \sqrt{L_r/C_{r1}+C_{r2}}$$

The capacitor voltages and inductor L_r current during this period are defined as follows:

$$\begin{aligned} V_{Cr1}(t) &= V_{bus} \cos(\omega_n t) \\ V_{Cr2}(t) &= V_{bus} - V_{cs} - V_{Cr1}(t) \\ i_{Lr}(t) &= I_o + \frac{V_{bus}}{z_n} \sin(\omega_n t) \end{aligned} \quad (14)$$

Once the $V_{cr1} = -V_{cs}$ and $V_{cr2} = V_{bus}$ the voltages will be clamped and the added energy in L_r will be transferred to C_s through $D_{s1,2,3,4}$. At time t_8 , the added energy in L_r has completely transferred to C_s and the current I_{Lr} equals I_o completing the stage. The approximate energy that was transferred into C_s from C_{r1} and C_{r2} equals

$$W_{cs_in2} = \frac{1}{2} \left[C_{r2} (V_{bus} + V_{cs})^2 + C_{r1} (V_{bus}^2 - V_{cs}^2) \right] \quad (15)$$

The current in L_{s2} reaches zero at time t_0 and L_{s1} will start conducting.

IV. ANALYSIS AND DESIGN

The advantage of the proposed soft switching methods for inverters is that they are passive so that no additional switches or control circuitry needs to be used. However, this passive nature means that the operation of the auxiliary circuit is dependent on the main switch operation and load current value. The component values therefore need to be designed to ensure soft switching and minimize the voltage stress across the switches under all circuit states. To summarize the design procedure, L_r and $C_{r1,2}$ are chosen to soften the switch turn on and turn off. $L_{s1,2}$ are chosen large enough to ensure soft switching over the complete load range but small enough to limit the switch voltage stress below the designed value. C_s is relatively large to store energy from cycle to cycle and control the ZCL energy, but small enough to provide soft switching under dynamic conditions. The design considerations apply to the full-bridge turn-on snubber inverter with current in the direction shown in fig. 7 and duty ratio D for switches S_1 and S_4 . The operation of the half bridge can be similarly derived with little modification. Additionally, the design considerations for an added turn-off snubber are given later. The operation in the opposite current direction has symmetrical equations and values.

A. Capacitor C_s voltage

The capacitor voltage is dependent on the size of the ZCL and ZVC and the output current level. For the turn-on snubber only, the capacitor voltage can be determined by examining the energy flowing into the capacitor from the ZCL and out of the capacitor by L_{s1} and L_{s2} . Equating (8) and (11) results in a quasi-static expression of capacitor voltage:

$$V_{cs} = \frac{2|I_o|\sqrt{L_s L_r}}{T_s \sqrt{(1-D)^2 + D^2}} \quad (16)$$

Here it is assumed that the output current frequency, F_o , is much lower than the switching frequency (i.e. $F_s/F_o > 100$). Later discussion will focus on the value of C_s and what happens at higher output current frequencies.

B. Minimum Capacitor C_s voltage

The capacitor voltage in (16) must be large enough to ensure soft switching over the complete load range. In order for soft switching to be maintained the switch transition period after S_1 and S_4 are turn off, t_{stp} , must be smaller than the off time of the switches.

$$t_{stp} \leq (1-D)T_s \quad (17)$$

Otherwise, $D_{s1,2,3,4}$ will still be conducting when S_1 and S_4 are turned on again and zero-current turn on will no longer be satisfied. Substituting (7) in (17) gives a minimum value for

the capacitor C_s . A symmetrical minimum capacitor voltage is found when current is negative.

$$V_{cs_min} = \frac{2I_o L_r}{(1-D)T_s} \quad I_o > 0$$

$$V_{cs_min} = \frac{-2I_o L_r}{DT_s} \quad I_o < 0 \quad (18)$$

C. Minimum L_{s1}, L_{s2} value

Setting (16) greater than (18) and setting $D = D_{max}$ results in a value for the snubber inductors with $L_s = L_{s1} = L_{s2}$.

$$\frac{L_s}{L_r} \geq 1 + \frac{D_{max}^2}{(1-D_{max})^2} \quad (19)$$

Equation (19) is a very important result. With a proper L_s/L_r ratio, soft switching is ensured regardless of the load or supply voltage.

D. Maximum Capacitor C_s voltage

The inductor L_{s2} was added to the synthesized results to create an automatic self-limiting feature on the capacitor C_s voltage. This can be seen by assuming L_{s1} and L_{s2} are uncoupled, and viewing the recovery circuitry as two interleaved buck-boost converters with C_s as the input source, V_{bus} as the output, and S_1 and S_3 as the switches. Under most conditions, they will operate in discontinuous inductor operation as was assumed with (16). However, when duty ratio is at either extreme (i.e. small or large), and the capacitor voltage is above a certain value, one of the inductors will enter continuous conduction mode of operation. In this mode, the inductor currents will increase until the capacitor voltage reaches a value so that the inductors are voltage second balanced. This places a maximum capacitor voltage level on the converters:

$$V_{cs_max} = \min\left(\frac{1-D}{D}V_{bus}, \frac{D}{1-D}V_{bus}\right) \quad (20)$$

Therefore, both (20) and (16) must be larger than the minimum capacitor voltage level, (18), for soft switching.

E. Maximum ZCL L_r value for soft switching

Setting (20) greater than (18) defines the largest value of L_r that can be used and still ensure soft switching.

$$L_{r_max} \leq \frac{(1-D_{max})^2}{D_{max}} \frac{V_{bus} T_s}{I_{max}^2} \quad (21)$$

Where I_{max} is the peak output current.

F. Determining C_s

The analysis assumed that although C_s was relatively large, its value was still small enough so that changes in output current would to allow the capacitor voltage to stay above

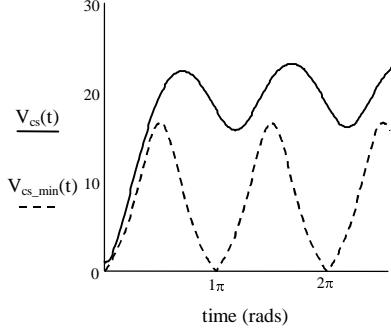


Fig. 9. $V_{cs}(t)$ for a step change in output power and frequency

V_{cs_min} . However, this places requirements on the value for C_s . What is needed, is to understand how the capacitor voltage will change in a dynamic condition or when the output current frequency increases with respect to the switching frequency. Circuit average modeling as explained in [22] provides a powerful and easy method. Assuming that the switching frequency is still more that 10 times the output current frequency, the average capacitor C_s voltage can be approximated from the average capacitor C_s current during each switching cycle.

$$\overline{V_{C_s}}(t) = \frac{1}{C_s} \int \overline{I_{C_s}}(t) dt \quad (22)$$

Where $\overline{I_{C_s}}$ is defined for the turn-on full-bridge snubber as

$$\begin{aligned} \overline{I_{C_s}}(t) &= \frac{W_{C_s_in1} - W_{C_s_out}}{V_{C_s} T_s} \\ &= \frac{2L_r \overline{I_o}^2}{V_{C_s} T_s} - \frac{\overline{V_{C_s}} T_s}{2L_s} (\overline{D}^2 + (1 - \overline{D})^2) \end{aligned} \quad (23)$$

With $I_o(t)$, $V_{cs}(t)$, and $D(t)$ all functions of time. Equation (22) is used to find C_s for the worst case condition when $I_o(t)$ is in phase with $D(t)$ and its frequency and power are maximized for a given system. Fig. 9 shows the theoretical dynamics of $V_{cs}(t)$ for a step change in load at an output frequency of 5kHz using the parameters from the 100kHz experimental system. In the figure, $V_{cs}(t)$ is always greater than $V_{cs_min}(t)$ maintaining soft switching.

G. Design with Turn-off snubber

Any soft turn-on full-bridge design that maintains soft switching over the complete operating range will also maintain soft switching with an added turn-off snubber as shown in Fig. 5a. Equation (15) shows that $C_{r1,2}$ adds a constant amount of energy into C_s each switching cycle. Therefore, the only design concerns are the added voltage stress across the main switches and the peak current through the switches when the capacitor is reset. The self-limiting feature of the circuit, even with a large turn-off snubber, still maintains a low C_s voltage. Quantitatively, the quasi-static capacitor voltage can be found by equating input and output

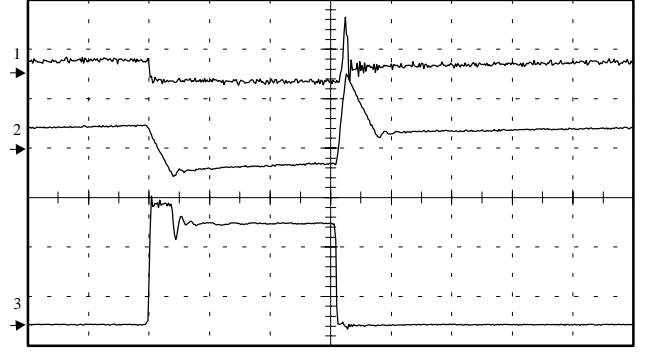


Fig. 10. Experimental waveforms: 1: I_{s2} , 20amps/div; 2: L_r , 20amps/div; 3: V_{ds2} ; 200volts/div; Horizontal scale: 10usec/div

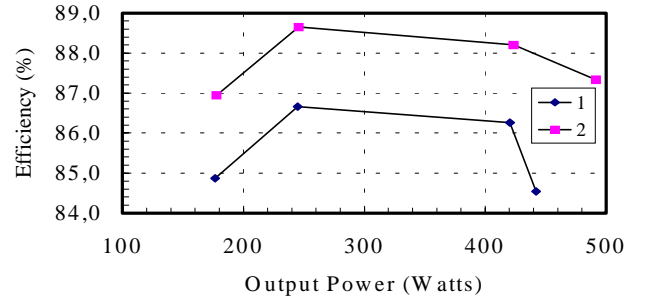


Fig. 11. Efficiency Tests at $F_o = 240\text{Hz}$; (1) Hard Switching; (2) Turn-on Snubber;

energy flow of the capacitor (i.e. $W_{inC_s_in1} + W_{inC_s_in2} = W_{inC_s_out}$) by using (8),(15), and (11). For higher frequency dynamics, (23) can be modified as follows:

$$\overline{I_{C_s}}(t) = \frac{W_{C_s_in1} + W_{C_s_in2} - W_{C_s_out}}{V_{C_s} T_s} \quad (24)$$

The peak switch current at turn on are found from (14) and equal:

$$i_{S1max} = I_o + \frac{V_{bus}}{2z_n} \quad (25)$$

V. EXPERIMENTAL RESULTS FOR SOFT TURN-ON FULL-BRIDGE EXAMPLE CIRCUIT

A 500-Watt experimental soft turn-on inverter was built to verify operations. IRFP460 MOSFETs were used as the main switches. Because MOSFETs do not have the current tail characteristic of minority carrier devices, the major losses are caused by the anti-parallel diodes at turn on. For this reason, the turn-off snubber version of the circuit was not used. The system parameters included: $F_s=100\text{kHz}$, $L_r=1.7\mu\text{H}$, $C_s=2\mu\text{F}$, $L_{s1}=L_{s2}=140\mu\text{H}$, and $L_{Lkg}=30\mu\text{H}$.

Fig. 10 shows the experimental waveforms for the voltage and current through switch S_2 . At turn off, notice how the voltage across the switch is clamped below 250volts until the

ZCL inductor changes polarity and finishes the switch transition period. At turn on, the voltage across the switch can drop well before the current increases, providing zero-current turn on. The current spike across the switch is caused by the reverse recovery of S_1 's anti-parallel diode and the charging of its drain to source capacitance.

Fig. 11 shows the improved performance the turn-on snubber provides over the hard-switched converter. It maintains more than 2% improvement over a wide power range at an output frequency of 240Hz.

VI. CONCLUSION

Promising lossless soft-switching full-bridge inverters were described that lower switch and diode stress and lower component counts compared to other previously proposed lossless inverters. A similar soft switching half-bridge was also shown. These inverters were examples from the results of a synthesis procedure for the creation of lossless passive soft switching converters. The synthesis procedure uses a set of properties to find all the *basic* soft switching topologies for a given converter. The *basic* soft-switching topologies described where the ZCL and ZVC are needed for soft switching. Then, a set of circuit cells is added to recover the energy in the ZCL and ZVC for lossless operation. Using a single ZCL, There are a total of 8 and 32 *basic* soft-switching topologies for the full-bridge and half-bridge inverters respectively. With the given circuit cells, several soft-switching inverters can be realized for each *basic* soft-switching topology. Other circuit cells are also possible, resulting in virtually limitless numbers of lossless passive soft-switching converters that can be created and this paper shows how.

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